High-Power Density DC-DC Converters Using Highly-Integrated Half-Bridge GaN ICs

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Abstract

This work develops high-power density DC-DC converters by combining monolithically integrated low-voltage half-bridge GaN ICs with two advanced packaging approaches. An in-house fabricated monolithically integrated half-bridge with application-specific gate width ratio is investigated. The half-bridge GaN ICs are assembled and compared using both PCB-embedding and flip-chip assemblies. Finally, DC-DC converters with a max. power of 30 W and power density of >1000 W/in^3 are realized by combing these GaN Power ICs and advanced packaging technologies.

1 Introduction

The power densities of low-voltage DC-DC converters in point-of-load (PoL) converters today range form 100-900 W/in^3 [1, 2]. The power density depends strongly on the output current. These PoL converters are required in small portable equipment. Especially for battery-powered devices, an increasing demand is predicted, driven by new battery applications such as wearables and drones [3]. PoL converters with Si-based power stages allow operation up to MHz switching frequencies. To further increase the switching frequency and the power density, GaN-based power semiconductors can outperform the state-of-the-art Si-based devices due to their superior figure-of-merits, and adapted packaging with reduced parasitics [1, 4]. In addition, GaN-on-Si high electron mobility transistors (HEMTs) are lateral devices that allow monolithic integration of multiple devices on a single die with a low-cost substrate.

One of the most commonly used topologies in low-voltage conversion is the half-bridge. There is already extensive work of monolithically integrated GaN half-bridges [5], which led to the commercialization of 100 V half-bridge GaN ICs several years ago [6]. For high step-down applications, asymmetric GaN half-bridges were developed. It has also been demonstrated that monolithic GaN half-bridges can be operated at higher voltages up to 400 V [7–9]. To get the best possible performance out of the device and the DC-DC converter, the package plays a key role. This requires advanced packaging techniques such as flip-chip or PCB-embedding, which fulfill the high requirements for electrical and thermal performance as well as compactness and reliability [10].

The approach of this work is to combine monolithically integrated half-bridge GaN ICs with advanced packaging technology for high-power density DC-DC converters. Fig. 1 illustrates the monolithic integrated GaN half-bridge with the GaN IC packaging.

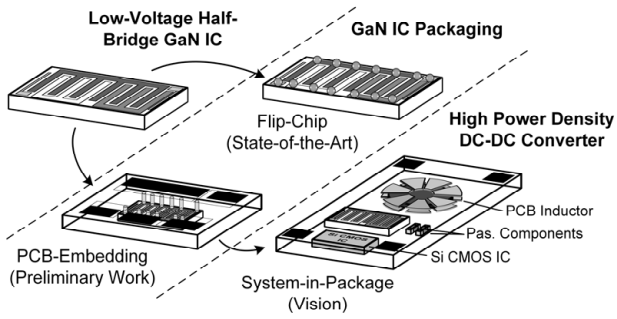

Fig. 1: Schematic illustration of combination of a half-bridge GaN IC with advanced packaging technology for high-power density DC-DC converters.

The design starts at device level and investigates the application-specific gate width ratio of the GaN half-bridge. At packaging level the two assembly techniques flip-chip and PCB-embedding are realized and examined. The design ends in a low-voltage high-density DC-DC converter demonstrator with separate PCB-embedded inductor.

2 Asymmetric GaN Half-Bridge

On device level, the design consists of the monolithic GaN half-bridge (HB) for low-voltage (LV) applications. The HB has two regions for the low-side (LS) and high-side (HS) transistors, shown in Fig. 2. A parameter for the HB design is the gate width ratio between the gate width of the HS and LS transistor $W_{G,HS/LS}$ given by: $k_G = W_{G,LS}/(W_{G,HS}+W_{G,LS}) = W_{G,LS}/W_{G,TOT}$. The gate width is inversely proportional to the on-resistance R_{ON}, and proportional to the area of the respective transistor. One objective is to calculate the optimal gate width ratio for buck converter with regard to the conduction losses. In addition, an in-house fabricated HB GaN IC (shown in Fig. 2) with special gate width ratio is described and characterized.

2.1 Optimal Gate Width Ratio

In many buck or boost converters a k_G = 50% is used due to the same HS and LS device selection, but this is not the best choice for many applications. In this context, the duty cycle *DC* of the LS conduction time during a switching period plays and important role. The duty cycle is given by $DC = V_{OUT}/V_{IN}$ for the buck converter in steady state in continuous conduction mode (CCM) and critical conduction mode (CRM).

The optimal gate width ratio is calculated based on the conduction losses $P_{COND} = R_{ON} \cdot I_{D,RMS}^2$ of the HB. The simplified calculation of the total conduction losses is given by:

$$P_{\mathrm{COND}} = I_{\mathrm{OUT}}^2 \left(R_{\mathrm{ON,LS}} \cdot DC + R_{\mathrm{ON,HS}}(1 - DC)\right), \quad (1)$$

consisting of the parts of HS and LS and depending of the output current I_{OUT} of the converter. The simplifications are I_D=I_L=I_{OUT}=const. and $L \to \infty$. The HS/LS on-resistance $R_{ON,HS/LS}$ is calculated by using the on-resistance scaled to the gate width R_{ON}' divided by the gate width $W_{G,HS/LS}$ of the HS/LS switch. The gate width of the HS/LS can in turn be described by the gate width ratio and the total

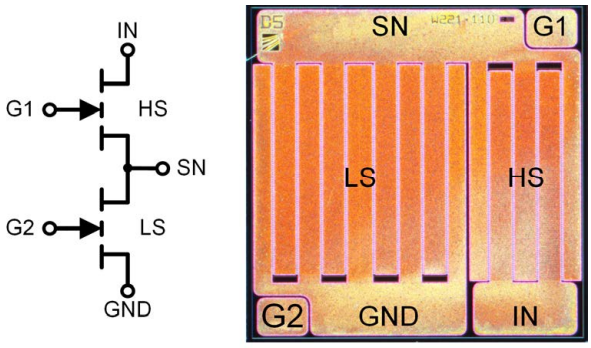

Fig. 2: Photography of a fabricated monolithic integrated low-voltage GaN half-bridge (2×2 mm²) with associated circuit diagram.

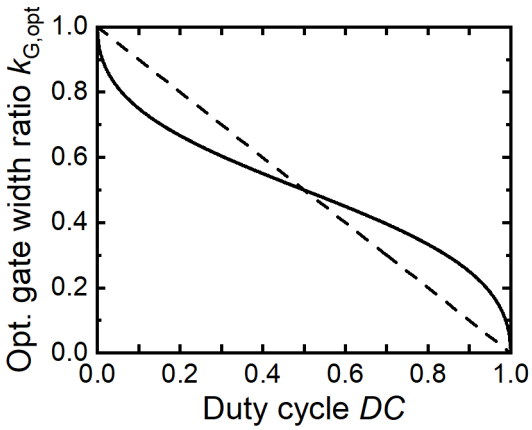

Fig. 3: Optimal gate width ratio $k_{G,opt}$ as function of duty cycle *DC*. The dashed line represents the non-valid linear relationship.

gate width $W_{G,TOT}$. To calculate the minimum conduction losses for a gate width ratio, the function must be derived and set to zero:

$$P_{\mathrm{COND}} = I_{\mathrm{OUT}}^2 \cdot R'_{\mathrm{ON}} \left(\frac{DC}{W_{\mathrm{G,TOT}} - W_{\mathrm{G,TOT}} \cdot k_{\mathrm{G}}} - \frac{1-DC}{W_{\mathrm{G,TOT}} \cdot k_{\mathrm{G}}}\right) \quad (2)$$

$$\frac{\partial}{\partial k_{\mathrm{G}}} P_{\mathrm{COND}}(k_{\mathrm{G}}, DC) = 0 \quad (3)$$

$$\Rightarrow k_{\mathrm{G,opt}} = \frac{\sqrt{DC - DC^2} + DC - 1}{2DC - 1}. \quad (4)$$

The function $P_{COND}(k_G,DC)$ represents the relationship between optimum gate width ratio and duty-cycle. In Fig. 3, k_G is shown as a function of *DC*. The analysis proves that the linear relationship $DC = 1\text{-}k_{G,opt}$ does not apply (see Fig. 3 dashed line). The optimum gate width ratio of 50% corresponds to a symmetrical half-bridge. If the converter operates with a different *DC*, the result is a different $k_{G,opt}$.

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However, not only conduction losses but also switching losses have a large contribution to the total losses in a buck or boost converter. At extreme gate width ratios k_G >95% or <5%, the relationship in equation (4) no longer applies because the max. saturation current of the smaller GaN HEMT decreases and the switching and conduction losses are affected [11].

Furthermore, the silicon-substrate termination of the monolithic GaN HB plays a decisive role. The backside of integrated HB either can be without connection (floating) or connected to a terminal of the HB (for example GND or IN), which influences the electrical parameters and also the thermal management [7–9, 11].

2.2 Half-Bridge GaN IC

The LV HB GaN IC is fabricated in a GaN-on-Si technology [12, 13] with a copper electroplating layer for compatibility with PCB-embedding technologies. The thickness of the copper layer is ~7 µm on the top and ~230 nm on the backside. The layout of each GaN HEMT is done in a matrix-structure, which is presented in [14]. This structure allows a low-resistance and area-efficient GaN device for LV power applications. The pitch between the fingers of the top copper metallization is 150 µm.

Fig. 2 shows a photography of the fabricated monolithically integrated GaN HB with matrix layout structure (chip area: 2×2 mm^2) and with the gate widths $W_{G,HS/LS}$ = 110/221 mm, which corresponds to a gate width ratio of ~2/3. With this gate width ratio, an optimal DC = 0.2 can be calculated with equation (2). Therefore, this gate width ratio is optimal for 5-to-1 V buck converter application. The LV HB GaN IC is characterized by a pulsed four-point measurement. Fig. 4 shows a measured output characteristic for the HS and LS GaN HEMT. The on-resistance R_{ON} is 33 mΩ for the HS and 16 mΩ for the LS HEMT. The area-specific on-resistance $R_{ON}{\cdot}A$ is ~0.44 mΩ·cm^2, including about 15% of the chip area reserved for pads (see Fig. 2, upper and lower parts of the chip) without active structure below. The on-resistance scaled to the gate width R_{ON}' is ~3.644 Ω·mm. The threshold voltage V_{TH} is -2 V, but can also be shifted to +1.8 V with the p-GaN gate module of our technology [15]. Fig. 5 shows the measured breakdown characteristic of both devices. The off-state leakage currents are measured up to 20 V. The drain leakage current is 181 µA (HS) and 412 µA (LS), which corresponds to a leakage current scaled to the gate width of

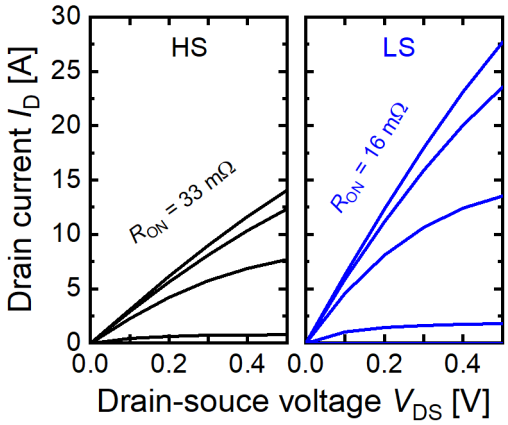

Fig. 4: Measured output characteristic (pulsed IV-curves with t_{pls} = 250 µs) for the HS and LS GaN HEMT.

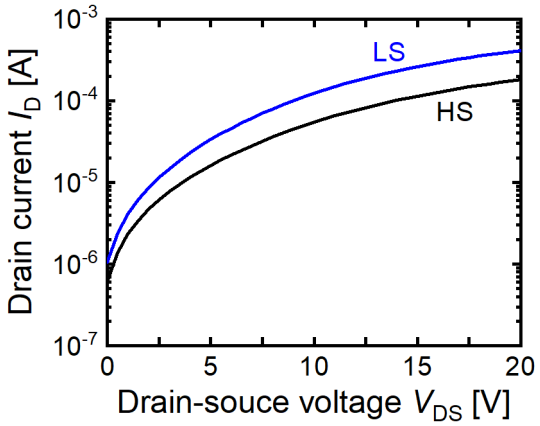

Fig. 5: Measured breakdown characteristic for the HS and LS GaN HEMT.

1.8 µA/mm. However, reduced drain leakage (by a factor of ~10-100) and gate leakage currents can also be achieved with the p-GaN gate module.

3 Packaging of the GaN IC

On the packaging level, a distinction is made between PCB-embedding and flip-chip assembly, as shown in Fig. 1. The HB GaN ICs are assembled using both packaging technologies. Subsequently, both advanced packaging technologies are described, compared, and advantages or disadvantages are highlighted.

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3.1 Flip-Chip Assembly

For the flip-chip assembly, 15 solder balls are manually placed on the GaN IC, shown in Fig. 6. The solder balls are NN2-SOL110-5C10SAH from TopLine®. These balls have an elastomer core and a special layer structure (plastic core/Ni/Cu/Ni barrier layer/Cu diffuse layer/SnAg solder/Ni dope) leading to a diameter of 110 µm. The solder ball is intended for a BGA pitch of 200 µm and the electrical ratings are <1 mΩ and <1.5 A. The balls were placed manually on the pads of the GaN IC (not on the active area) with solder flux and then soldered to the IC in the refow oven with a specially adapted soldering profile [16]. An automatic placement of the solder balls on the active area of the transistor is also conceivable with a smaller diameter and a solder jetting automat. Solder jetting has the advantage of flux free soldering by laser, solder ball size from ≥40 µm, solder ball speed >3 balls/s, and rework capability on wafer as well as chip level [17]. The GaN ICs with the solder balls are soldered onto the main converter PCB in a further soldering step.

3.2 PCB-Embedding

The GaN ICs are embedded using the ECP® - Embedded Component Package Technology from AT&S, as shown in Fig. 7. Using an adhesive film, the GaN IC is placed and fixed in the core of an FR-4 (4×4 mm^2) within a pre-cut cavity. To permanently connect the dia with the PCB structure a prepreg is laminated on top of the structure while the adhesive tape is removed this process step. In the next production steps, 12 VIAs to the GaN IC with a diameter of 100 µm of the outer structured 35 µm thick copper layer are realized in the 4-layer structure [18]. Furthermore, the technology allows contacts to the die from both sides, which in our case could also be used as thermal VIAs for heat dissipation via the back side. In total 48 ICs were embedded on 8 cards with 6 ICs each. After optical x-ray scanning, a yield of 96% was achieved. The measurements from Fig. 4 and Fig. 5 were performed after PCB-embedding. The embedding method yields the advantage of the integration of further dies in the same package, as planar inductors [18, 19], transformers [20], gate drivers and DC link capacitors [21] to increase the power density of the overall system. The PCB-embedded GaN ICs are soldered onto the main converter PCB in a further soldering step.

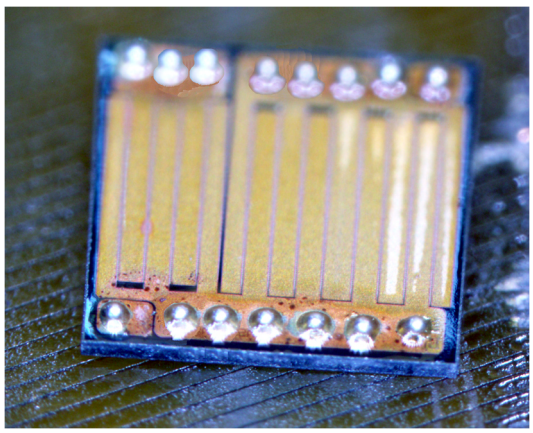

Fig. 6: Photography of the GaN IC with manually flip-chip assembly.

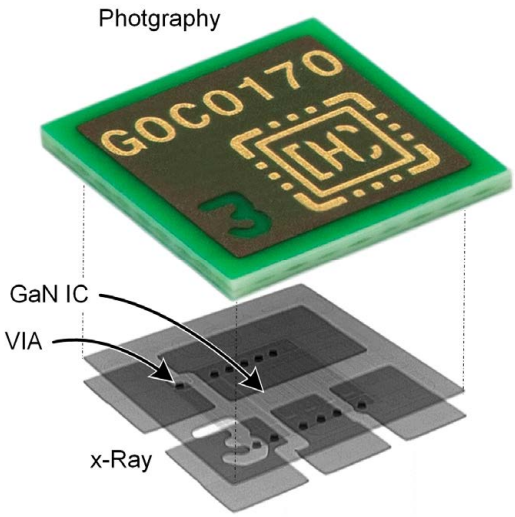

Fig. 7: Photography and x-ray image of the GaN IC embedded in a PCB (4×4 mm^2) with the AT&S's ECP® - Embedded Component Package Technology.

Tab. 1: Comparison between flip-chip assembly and PCB-embedding

	Flip-Chip Assembly	PCB-Embedding
Resistance [mΩ]	≤1/ball	<0.15/VIA
Diameter [µm]	110/ball	100/VIA
Min. Pitch [µm]	200/ball	160/VIA (1)
Yield	-	High
Heat dissipation	Low	High
Cost	Medium	High

(1) same net, component area only

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3.3 Comparison

Tab. 1 compares the most important parameters of both packaging technologies. The advantage of flip-chip assembly is that no additional carrier substrate is required, and therefore the power stage packaging is not increased compared to conventional packages. Heat dissipation is the problem with such chip scale packaging, since only the heat can be transported via the electrical contacts and the air. It is also difficult to attach a heat sink to the backside. In this point, the PCB-embedding has a clear advantage. The heat can be dissipated better through thermal VIAs at the backside. The realized PCB-embedded package can further be improved by thermal VIAs to the backside, then a thermal resistance of <1 K/W can be achieved with corresponding diameter and pitch according to [10]. From the point of view of electrical contacting, there are no advantages or disadvantages with the respective technology. However, the solder balls or the VIAs were placed on the pad areas of the GaN IC, which are actually intended for bond wires. These pad areas could be removed to increase the area-specific on-resistance and the chip could be directly connected on the active area. In case of hermetic isolation, the PCB-embedding has significant advantages. If flip-chip ICs are exposed to moisture or other contaminants, it is mandatory to us an additional underfill.

4 High-Power Density DC-DC Converter Demonstrator

This design from device to packaging was verified in a high-power density DC-DC converter, which is shown in Fig. 8. Not only power semiconductors play a decisive role, but also magnetics. In many DC-DC converters, the magnetics are typically the largest components. Therefore, there is a high demand for miniaturized power inductors with low losses and high flux densities [2]. In the following, the design of the converter and the PCB-embedded inductor will be described. A detailed characterization of the DC-DC converter will also be performed. Finally, the performance of the LV DC-DC converter is classified according to the state-of-the-art.

4.1 Design

The main components of the DC-DC converter demonstrator are the LV HB GaN IC and a PCB-embedded planar inductor. These components are connected as synchronous buck converter. The HB is driven by the high-speed GaN FET driver PE29101 from pSemi. The dead time can be adjusted via two resistors and the gate resistors for the HS and LS switch have the values 4.7/2.2 Ω (pull-up/-down resistor). A function generator provides the PWM signal. A special feature is the bipolar bootstrap circuit similar to [22], which can be used for d-mode GaN HBs. The connection pads for the GaN HB are suitable for the two flip-chip assembly and PCB-embedding variants. Finally, the DC link capacitors for the input and output have a value of 6.7 µF.

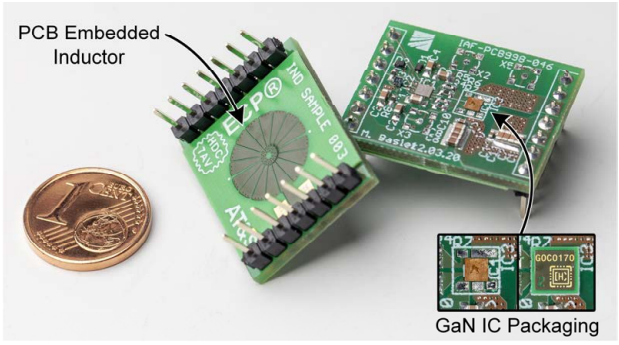

Fig. 8: Photography of the high-power density DC-DC converter demonstrator with the two presented GaN IC packages and PCB-embedded inductor.

A planar embedded inductor of [19] was used in the DC-DC converter, shown in Fig. 8. This inductor was embedded with the same technology from AT&S as the GaN Power IC. For this purpose, a magnet core was positioned in the center instead of the GaN IC, which was cut into the desired shape with a laser [18]. The magnetic material is based on flakes to reduce the effect of eddy currents. Toroidal windings around the magnet core are realized with two copper layers and plated VIAs [19]. The use of the same technology allows the fabrication of all major components in a single PCB process and can result in an enormous cost advantage, especially compared with coiled inductors. Embedding of both furthermore reduces parasitics, which in turn allow to increase the switching frequency further. The embedded inductor was fabricated with/without air gap, an inductance of 2.2/5.7 µH, and a self-resonance frequency of 40/30 MHz. The inductor with air gap has a rated DC current of 2 A and a DC resistance of 75 mΩ. Both inductors have 16 turns and an outer diameter of 10.5 mm.

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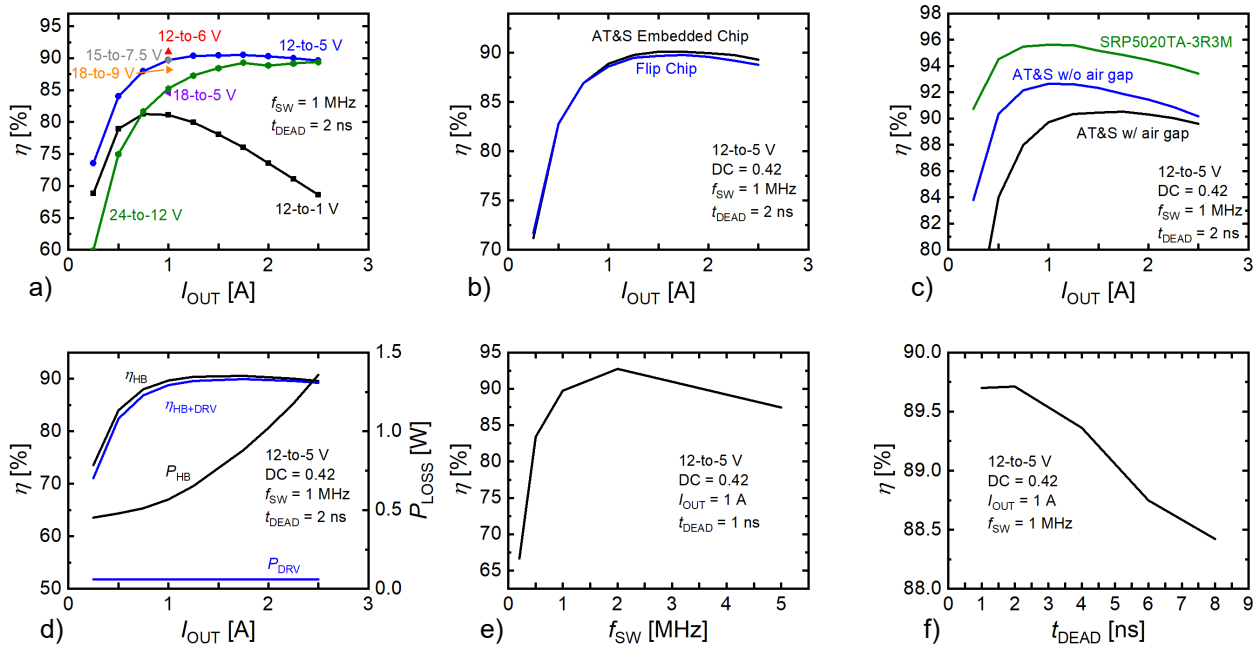

Fig. 9: Measured efficiency η as function of the input current I_{OUT} with a) different duty-cycles, b) two packaging technologies, c) different inductors, d) comparison between half-bridge with and without driver as well as corresponding losses P_{LOSS}, as function of switching frequency f_{SW}, and as function of the dead time t_{DEAD} for the high-power density converter demonstrator.

4.2 Measurements

Different parameter variations were carried out in numerous measurements. The purpose was to measure the HB GaN IC in combination with the inductor up to its current limit in order to achieve a maximum power density. The efficiency was measured in controlled PWM operation and the converter was connected to an electronic load in constant current mode.

Fig. 9 shows the characterization with parameter variations. All measurements except Fig. 9 c) were performed with the embedded inductor without air gap. The measurement in Fig. 9 a) investigates the influence of different duty cycles. The highest efficiency of 91% is achieved with the 12-to-6 V conversion, instead of the 18-to-5 V, due to a large current ripple caused by a low inductor inductance. The 18-5 V conversion results in a $DC = 0.28$ and corresponds to a $k_{G,opt} = 0.62$. This is closest to the used gate width ratio of 2/3. It shows also that for extreme duty cycles (e.g. $DC = V_{IN}/V_{OUT}$ = 1 V/12 V = 0.083) with higher output currents a low efficiency is achieved. The impact of IC packaging is measured in Fig. 9 b). Up to an output current of 0.75 A both efficiencies are similar for low currents, then with higher currents the efficiency of PCB-embedding is insignificantly higher. It is very likely that the thermal performance of PCB-embedding is better with large pads. However, the thermal management of both versions can be improved with thermal VIAs or heat sinks. Therefore, the packaging level can also be optimized in the design. Different inductors investigated in the measurement are shown in Fig. 9 c). Higher efficiencies have been achieved with a conventional inductor, but the PCB-embedded inductors are still in the development phase and further optimization can improve the parameters of the inductor. Fig. 9 d) shows the measurement of the efficiency and losses with (HB+DRV) and without (HB) gate driver losses. The losses of the gate driver are ~60 mW, and have not been particularly optimized. The measurement in Fig. 9 e) and f) illustrates the efficiency as a function of the switching frequency and dead time. An optimum can be determined at 2 MHz and a dead time of 1-2 ns.

4.3 State-of-the-Art of Point-of-Load Converters

The volume of the DC-DC converter is determined to be 12×12×2 mm^3 for both

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packaging techniques to calculate the power density. With a max. output current of 2.5 A and a max. output voltage of 12 V (see Fig. 9 a)), the max. output power of 30 W resulting in a power density of ~1707 W/in^3 or ~104 W/cm^3 is achieved, which demonstrates that the combination of monolithic and package-level integration approaches can achieve high-power densities. Commercial products also already exceeded the limit of 1000 W/in^3 with a output power of ≤15 W [23]. The power density limit for PoL converters is currently at 1 W/mm^3 at the maximum, which was achieved by a system-in-package (SiP) with high performance power semiconductors realized in a kind of PCB-embedding [23]. Industry is leading over research in terms of power density due to commercial products with optimized volume and efficiency driven by cost pressure.

5 Conclusion

A design of high-power density DC-DC converters with optimized gate width ratio of monolithically integrated GaN half-bridges is presented. The monolithically integrated half-bridge dies are packaged in two assembly technology variants for comparison. The embedded GaN ICs in combination with inductors shows the compatibility of the GaN technology with the PCB-embedding technology. Using these GaN power devices, converters with high-power densities >1000 W/in^3 can be achieved.

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