GaNonCMOS H2020 Research:

Sub-25V Switch Technologies for use in PwrSiP and PwrSoC

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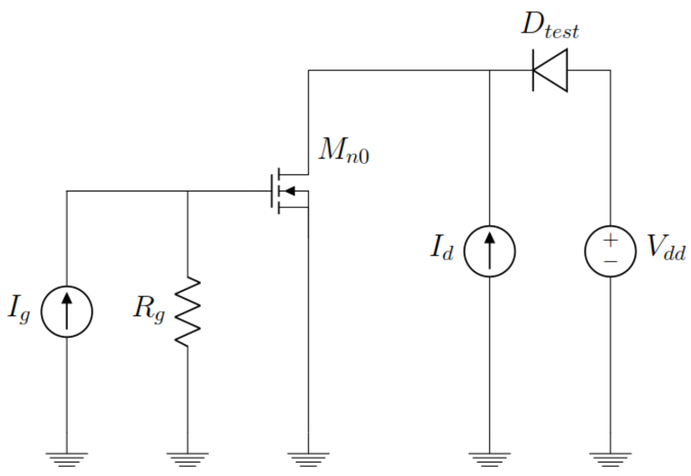
Abstract

The movement toward higher integration onto silicon has led to a renewed focus on switching performance in low-voltage non-isolated point-of-load (POL) power converters. A range of semiconductor switches are characterised using several standard and custom figures of merit (FOMs) based on gate charge, on-resistance and switch area. Tested devices include those from 180 nm Silicon-on-Insulator (SOI) processes, bulk CMOS processes at 65nm and 28nm, and discrete devices such as GaN e-HEMTs, Trench VDMOS and planar LDMOS. Cascode arrangements of multiple lower-voltage switches are compared against their single high-voltage switch equivalents.

Methodology

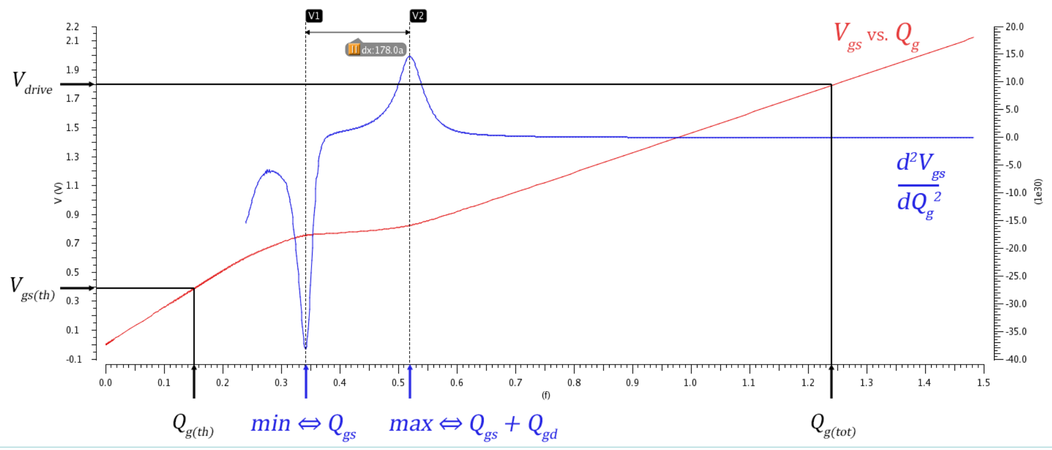
Fig. 1. Test circuit for characterisation of single NMOS (top) and cascode PMOS (bottom) switches



Integration of the gate drive current I_g yields the accumulated gate charge Q_g, against which V_{gs} is plotted as shown below. The gate is charged through its threshold voltage $V_{gs(th)}$ and Miller plateau ($\Delta V_{gs} = {}^{I_{ds}}/_{g_m}$) to a specified drive voltage. These points are used to measure $Q_{g(th)}$ and $Q_{g(tot)}$.

A novel method is proposed for extracting gate charge points corresponding to the start and end of the Miller plateau using the second derivative of drive voltage $\frac{d^2V_{gs}}{dQ_g^2}$. This allows automated measurement of Q_{gs} and Q_{gd} in simulation.

Fig. 2. Extraction of gate charge characteristics from simulation waveforms



Results & Discussion

- Degradation in switching FOM with finer geometry for 1V2 and 1V8 sample devices.
- Core voltage devices for given process geometry exhibit superior performances than devices with non-core rating.
- Cascodes: 3 X 1V8 (≡ 5V4) on 180nm SOI exhibit better switching FOM but poorer Specific R_{dson} than equivalent single device.
- Distinct advantage in discrete GaN e-HEMT @ 15V vs (3 X 5V 180nm SOI): 39 vs 300 mΩ.nC.
- GaN e-HEMT performs comparably to Trench VDMOS and LDMOS at 25/30V.

Fig. 3. High-Frequency Switching Capability versus Device Voltage Rating

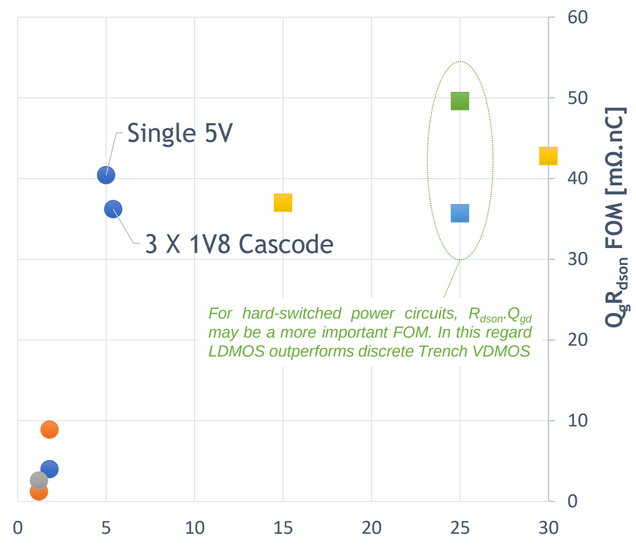
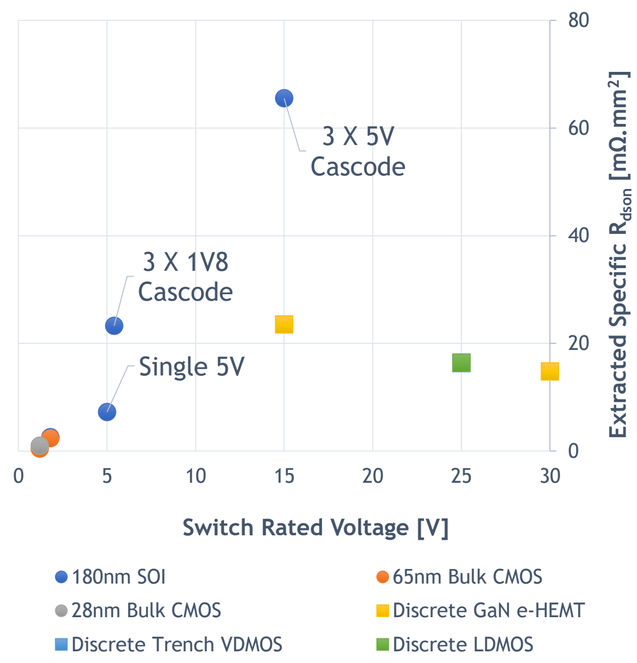


Fig. 4. Extracted Specific On-Resistance versus Device Voltage Rating



Notes: The chart in Fig. 3 shows results of simulations using the test circuits shown in Fig. 1. Note that the FOMs associated with the discrete NMOS devices (square markers) have been normalised for comparison with the integrated PMOS devices (circular markers) by assuming a 2X mobility difference between P and N.

Conclusions & Future Work

- A simulation-based method of characterising the switching performance of integrated devices was developed, to extract FOMs similar to those used in the discrete switch industry.
- High-performance integrated switches may be optimally created by using cascodes of a node's core devices. This approach requires additional area/complexity in level shifters, gate drivers and additional stacked voltage rails.
- The characterisation of cascodes leads to the suggestion for new energy based switching FOMs (as opposed to charge based) e.g. $E_g.R_{dson}$ vs $Q_g.R_{dson}$.
- The next stage of this work involves simulations of cascode *hot well* charge injections through the various well to substrate junction capacitances and comparison with SOI.

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