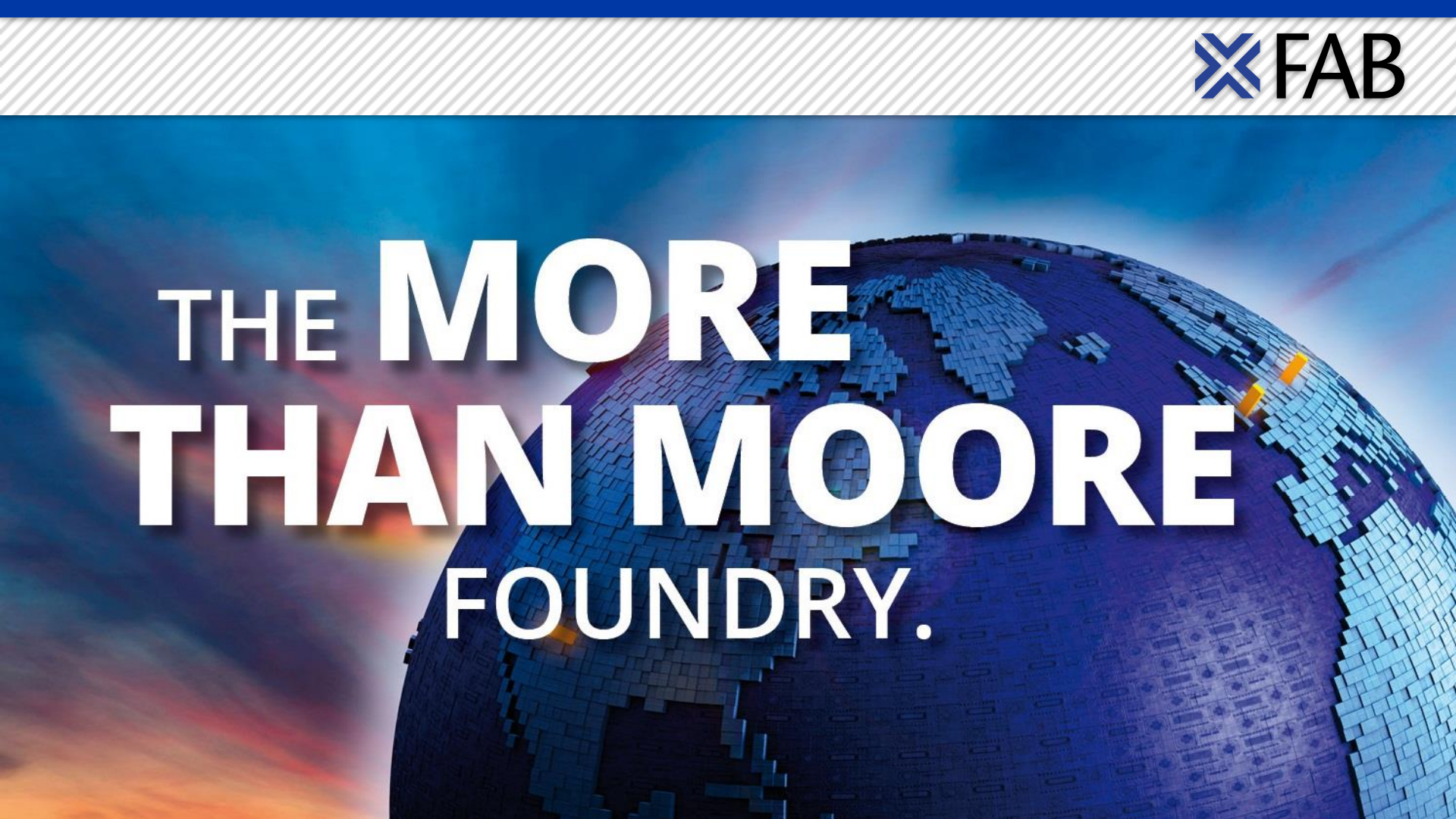

FAB
THE MORE THAN MOORE
FOUNDRY.

GaN and CMOS integration

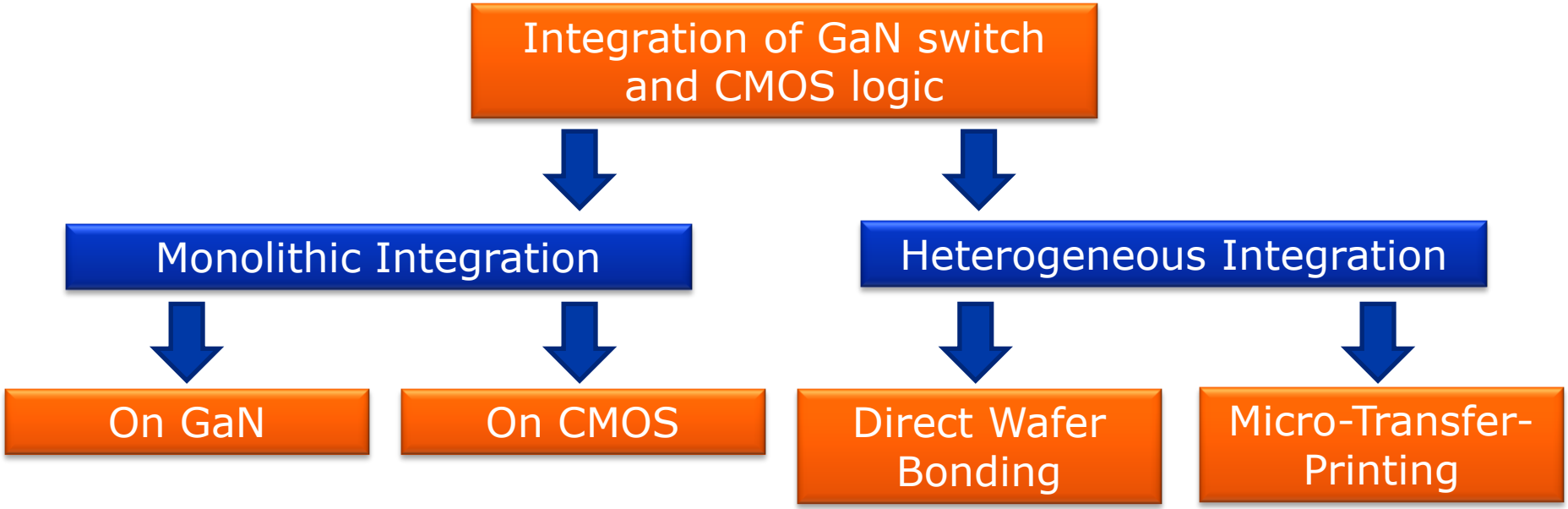
Ralf Lerner

Summer school on wide-bandgap nitride devices, July 2019

With some results from

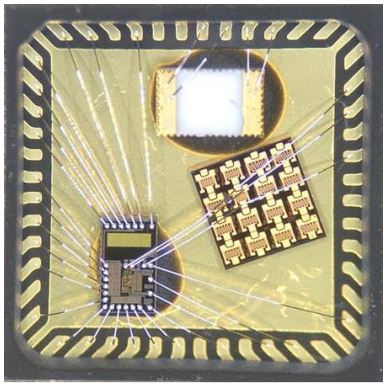
as well as from literature and other projects

Integration variants GaN and CMOS on wafer level



In contrast to

- System in package (SiP): a number of ICs or chips are mounted in a single carrier package. Dies may be arranged horizontally or stacked vertically on a substrate, internally connected by
  - Wire bonds
  - Flip chip technology e.g. solder bumps
  - Vertical connections e.g. by Through Silicon Vias (TSV)
- SiP contains several chips (processors, memories, opto-electronics) on the same substrate – resulting in functional package unit
  - No or few external components need to be added to make it work
  - Particularly valuable in space constrained environments like mobile phones
  - Reduced complexity of printed circuit board (PCB)
  - Critical yield issue: any single defective chip in the package will result in a total fail (even if everything else works fine)



Picture: Turck Duotec, MIIMOSYS project

Content

- Introduction
- Monolithic integration on GaN
- Monolithic integration on CMOS
- Integration by wafer bonding
- Heterogeneous integration by micro-Transfer-Printing
- Summary

Introduction

Who we are

The More than Moore Foundry.

- 25+ years of experience in pure-play foundry services for analog/ mixed-signal semiconductor applications
- Specialty foundry with a comprehensive set of technologies serving various market segments

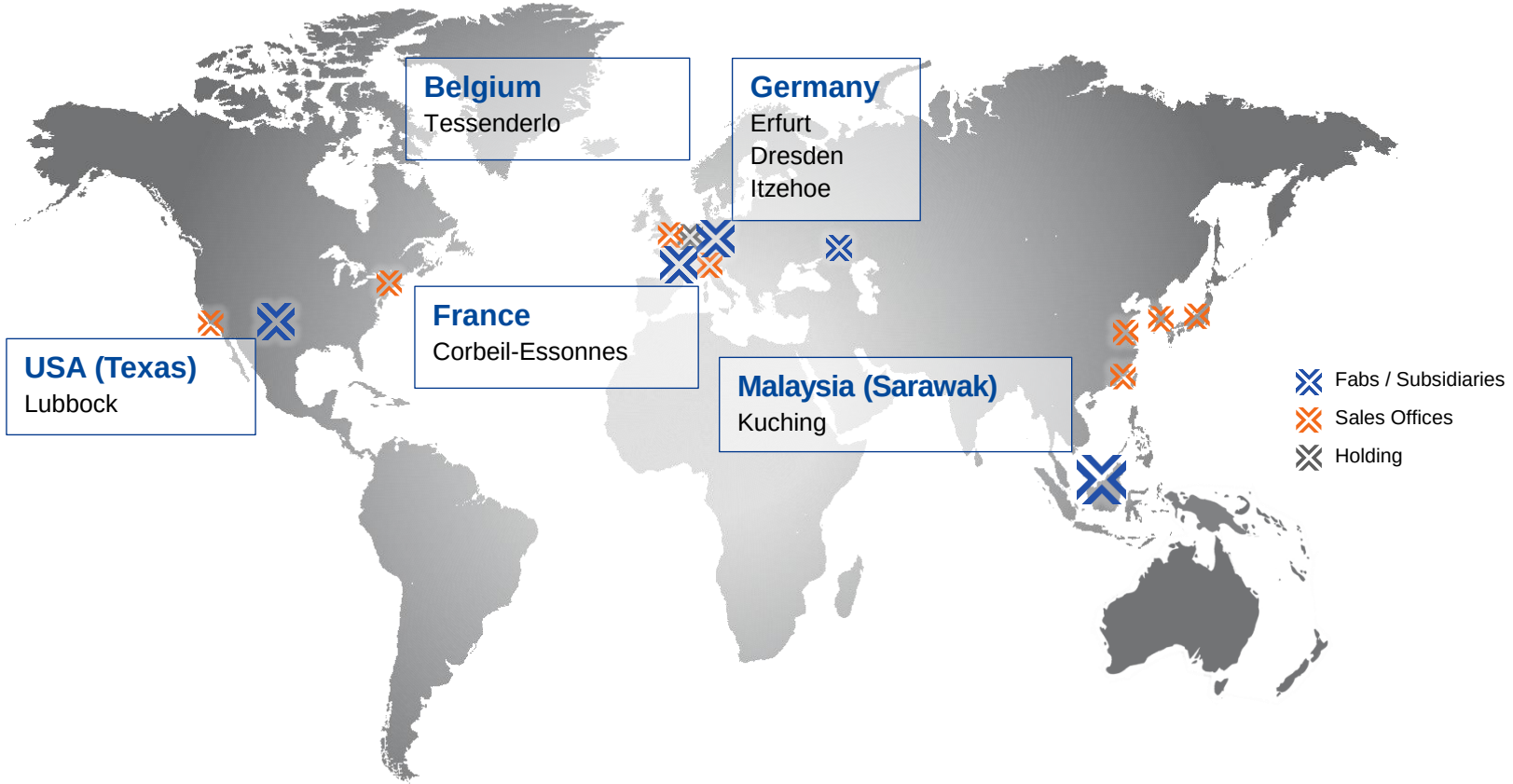
Technologies interfacing the real world

- Expertise in analog/mixed-signal IC production, MEMS and SiC with a focus on high-growth automotive, medical and industrial end markets with long lifecycles
- Strong design support to drive customer engagement over the long-term with successful technology leaders

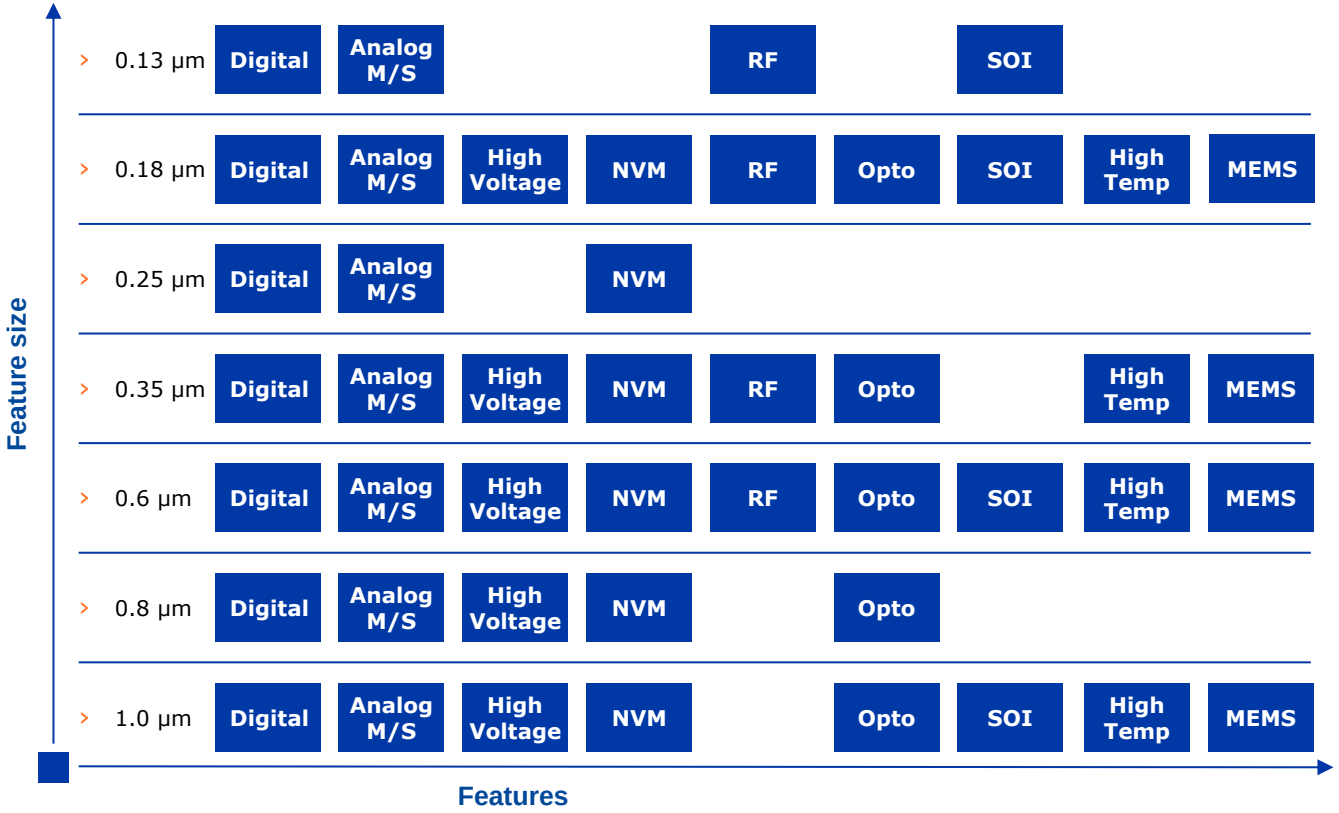
Manufacturing excellence

- 6 wafer fab facilities in Germany, France, Malaysia and US
- Capacity: 98,000 wafer starts per month (200 mm equiv.)
- All production sites are automotive qualified
- About 4,000 employees worldwide

Location | X-FAB Worldwide



Open-Platform Technology Offering



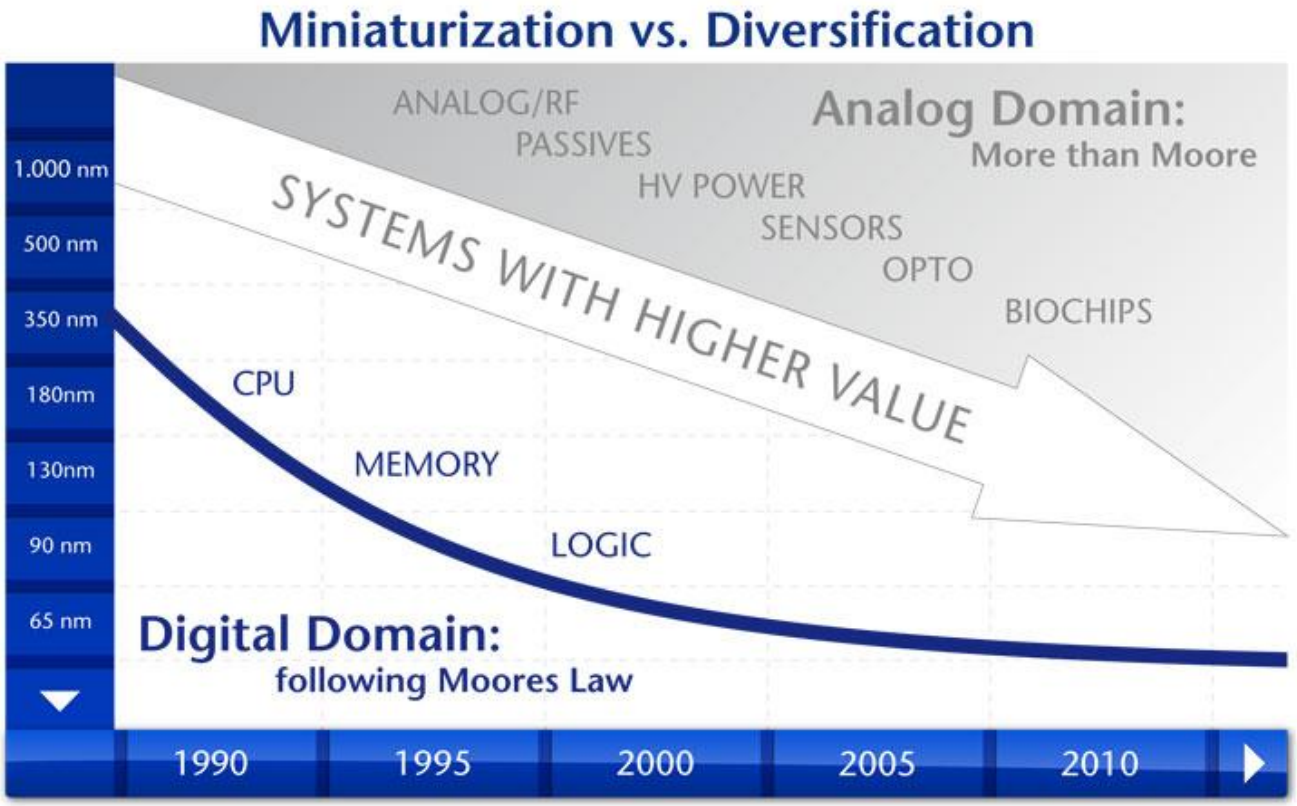
M/S = Mixed-Signal, NVM = Non-Volatile Memory, RF = Radio Frequency, SOI = Silicon On Insulator

Broad product range

- X-FAB owns technology and corresponding IP
- Extensive IP offering; ability to customize IP
- Modular approach to tailor to your needs

Explore X-FAB's large portfolio of CMOS & SOI processes online

More than Moore



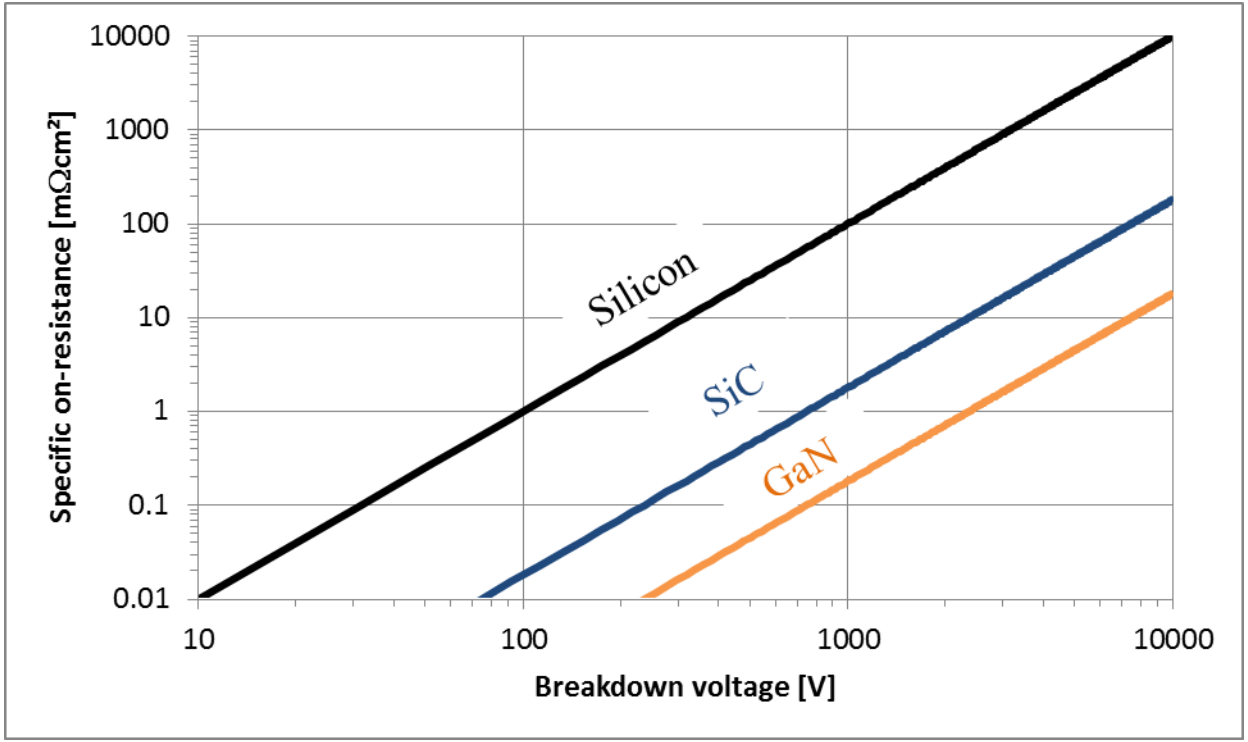
Motivation for GaN & CMOS integration

- Superior GaN performance as fast power switch & CMOS logic with high functionality
- Reduced interconnect distances and losses – both affecting performance
- Smaller form factor
- Reduced power consumption
- Lower cost
- Lower complexity in assembly

K. H. Lee et al, Monolithic integration of III–V HEMT and Si-CMOS through TSV-less 3D wafer stacking, 2015 IEEE 65th Electronic Components and Technology Conference (ECTC)
Zhu, Matioli, Monolithic integration of GaN based NMOS Digital Logic Gate Circuits with E-Mode Power Gan MOSHEMTs, ISPSD 2018

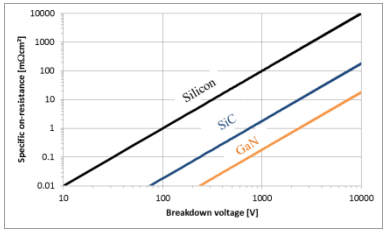
Bringing together GaN

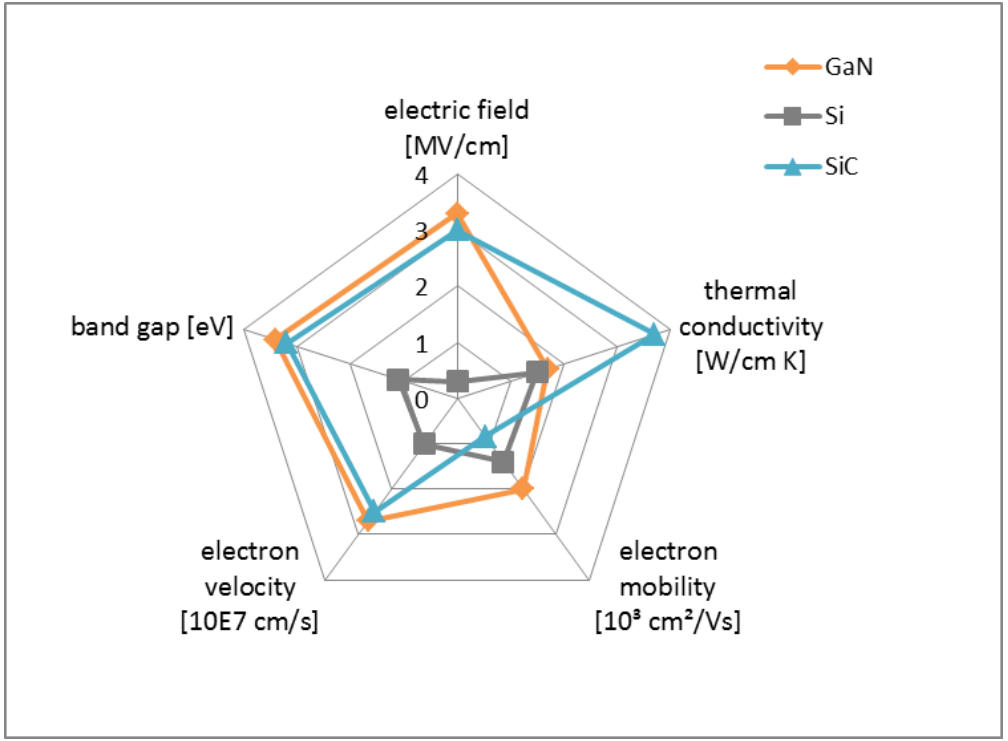
- superior performance: on-state and switching



Bringing together GaN

- Superior material parameters

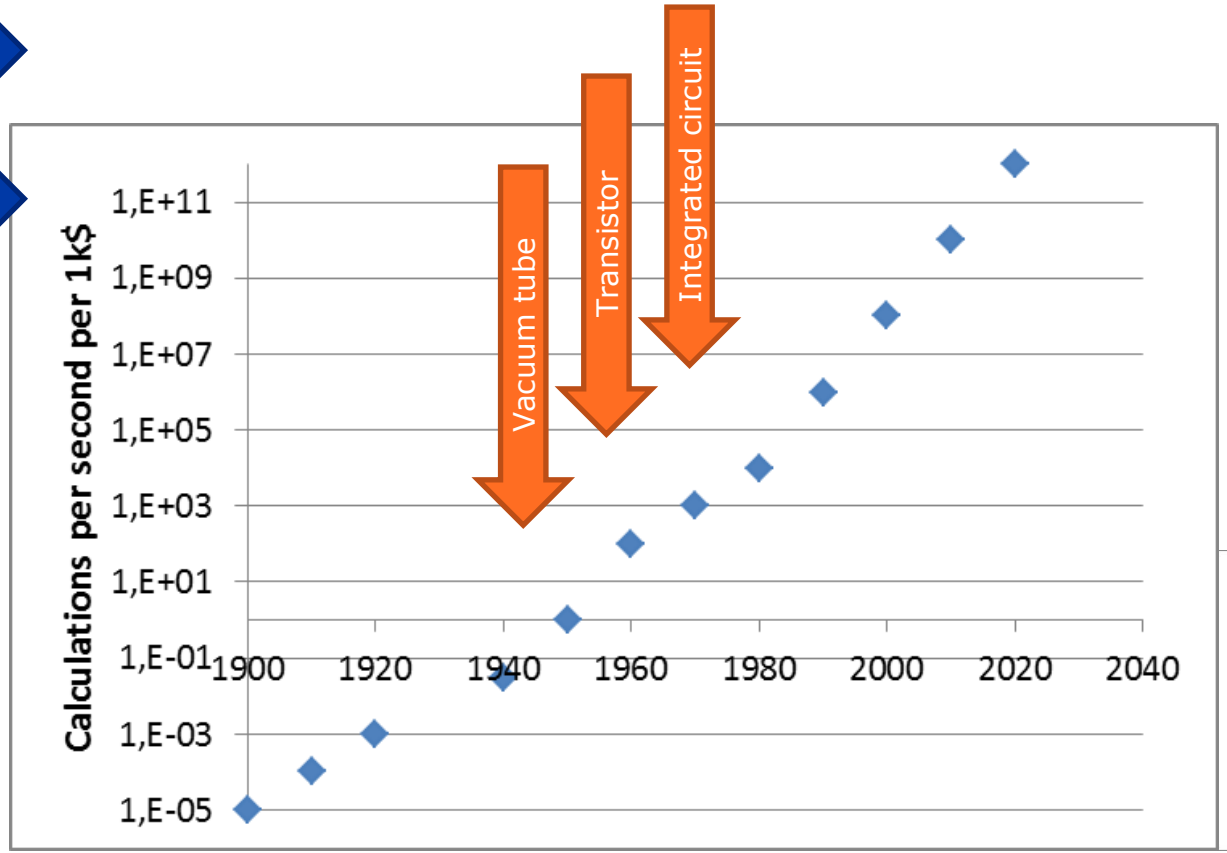


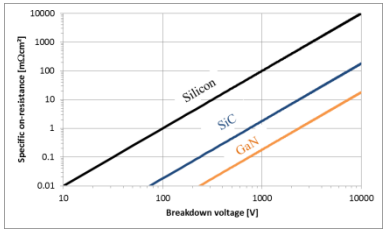


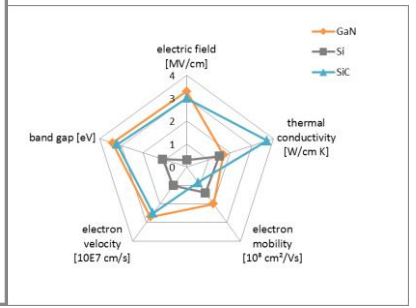
Bringing together GaN and CMOS logic

Human brain

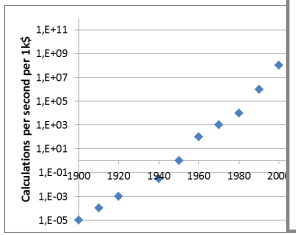
Mouse brain

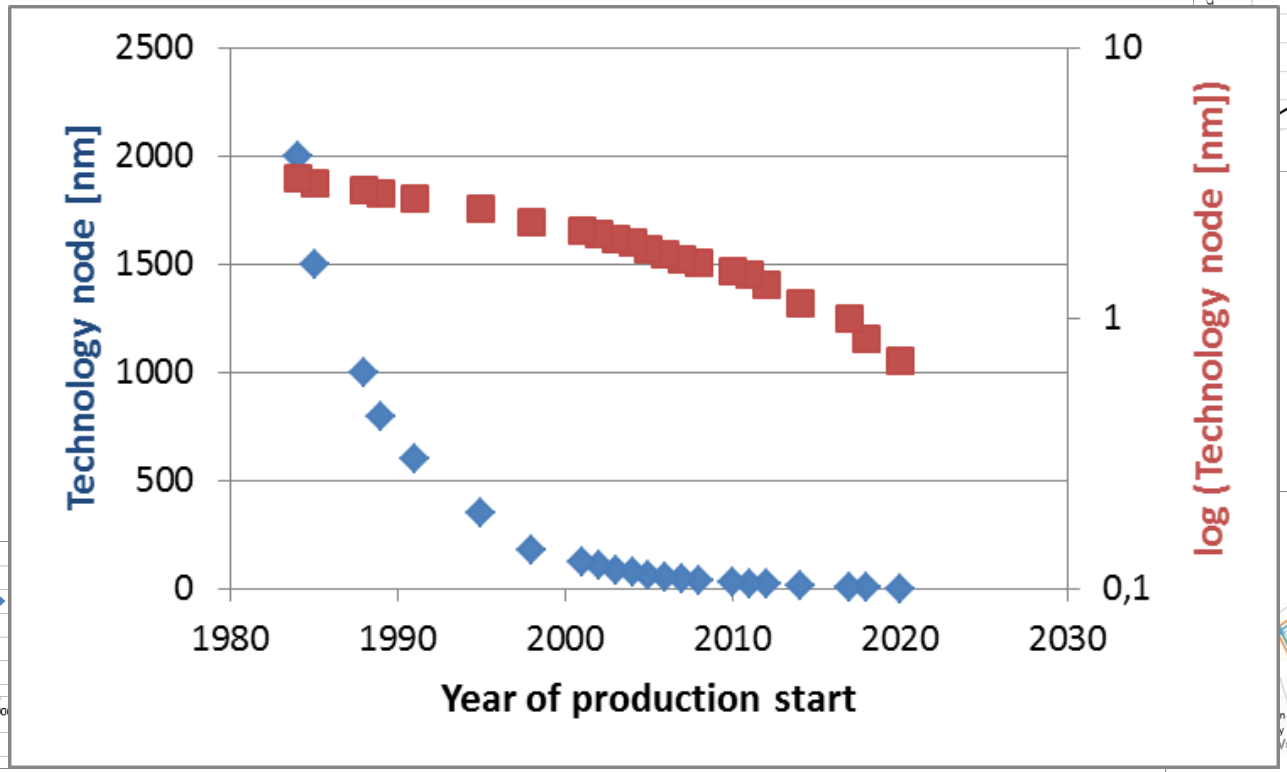


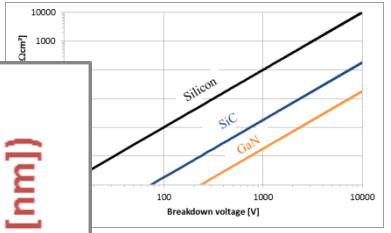


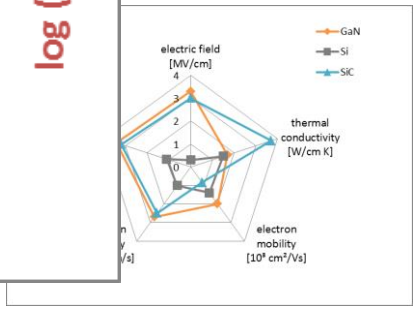


Bringing together GaN and CMOS logic



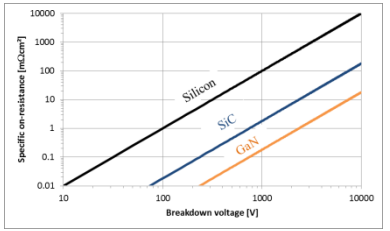


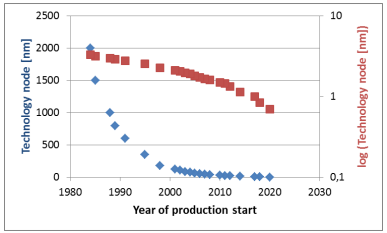


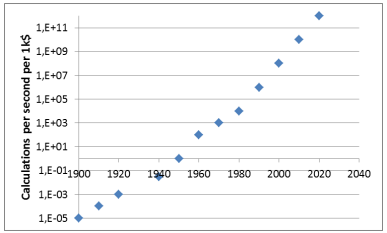


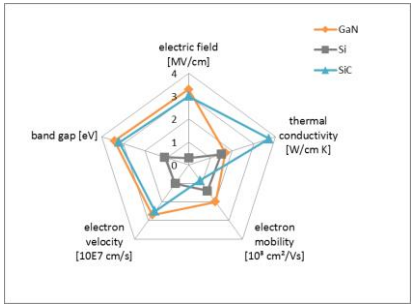
Bringing together GaN and CMOS logic

- Means
- A combination of incredible logic complexity just about to beat human brain
- With a very fast switch with low losses







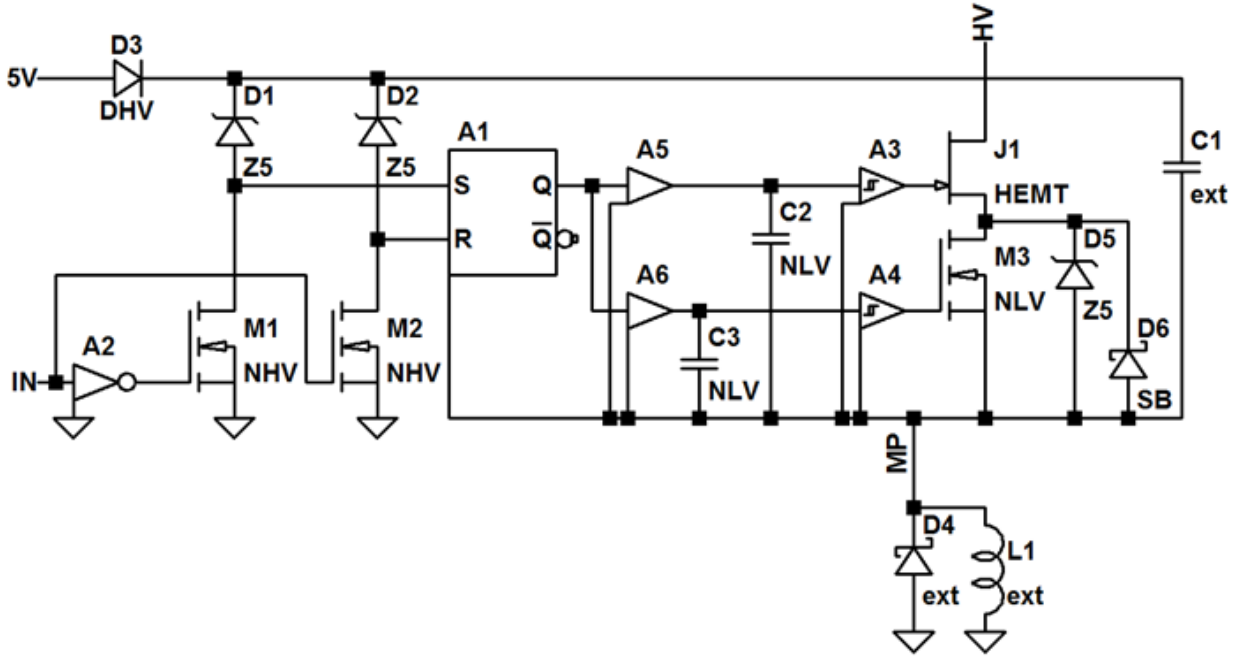


Difficulties

- Combination of different semiconductors with different properties
  - Mismatch of crystal structure and lattice constants
  - Different coefficients of thermal expansion
  - Growth temperatures versus temperature stabilities
- Electrical requirements
  - Low parasitic inductances
  - Isolation
- Other
  - Heat removal
  - Wafer diameter
  - Costs of semiconductor

Example for GaN & CMOS integration

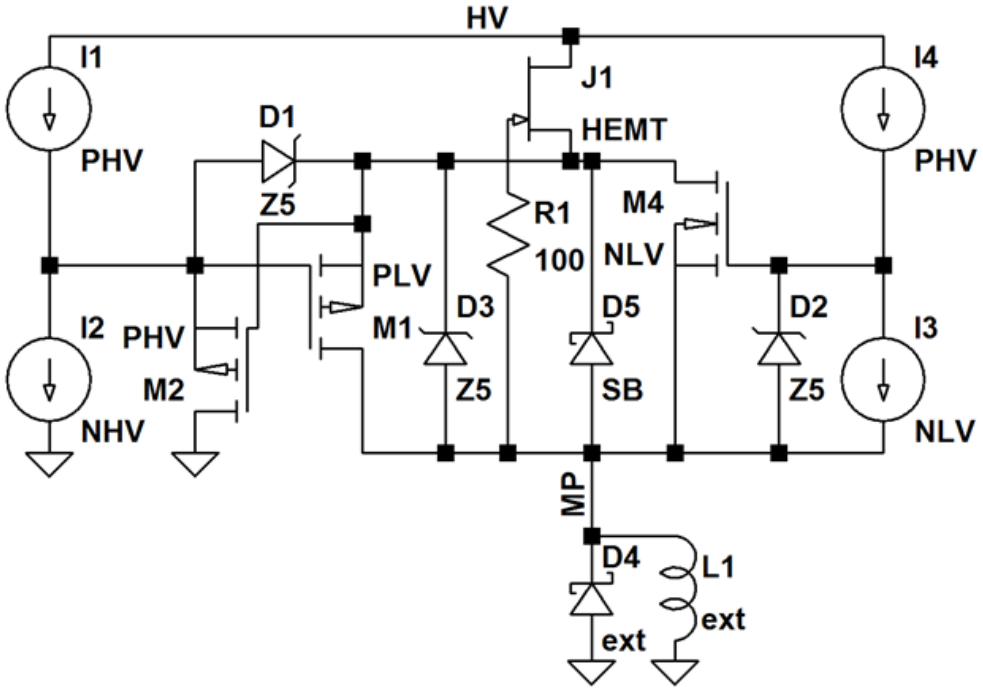
- Example from MIIMOSYS project: bootstrapped GaN motor driver



Courtesy: Electronic Design Chemnitz

Example 2 for GaN & CMOS integration

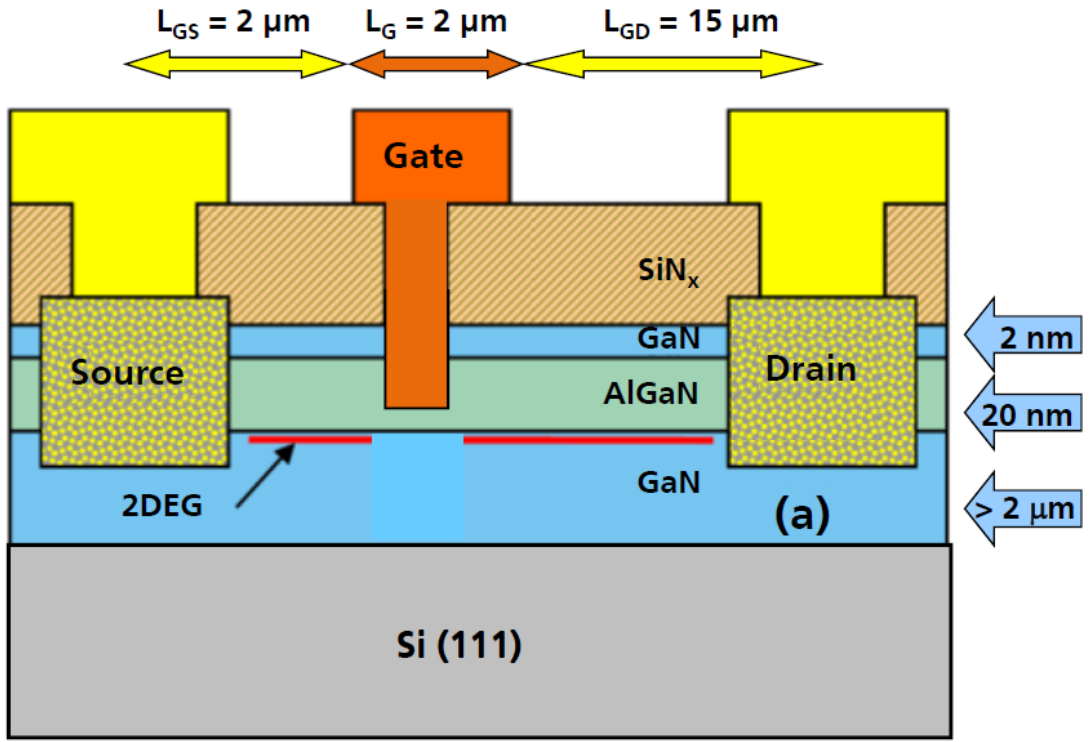
- Example from MIIMOSYS project: static motor driver



Courtesy: Electronic Design Chemnitz

HEMT

- Schematic cross section of a High Electron Mobility Transistor, HEMT
- Measures of Power device:
- For RF:
  - LG ≤ 350nm
- Lateral structure:
  - Drawbacks for current supply
  - But big advantage for integration



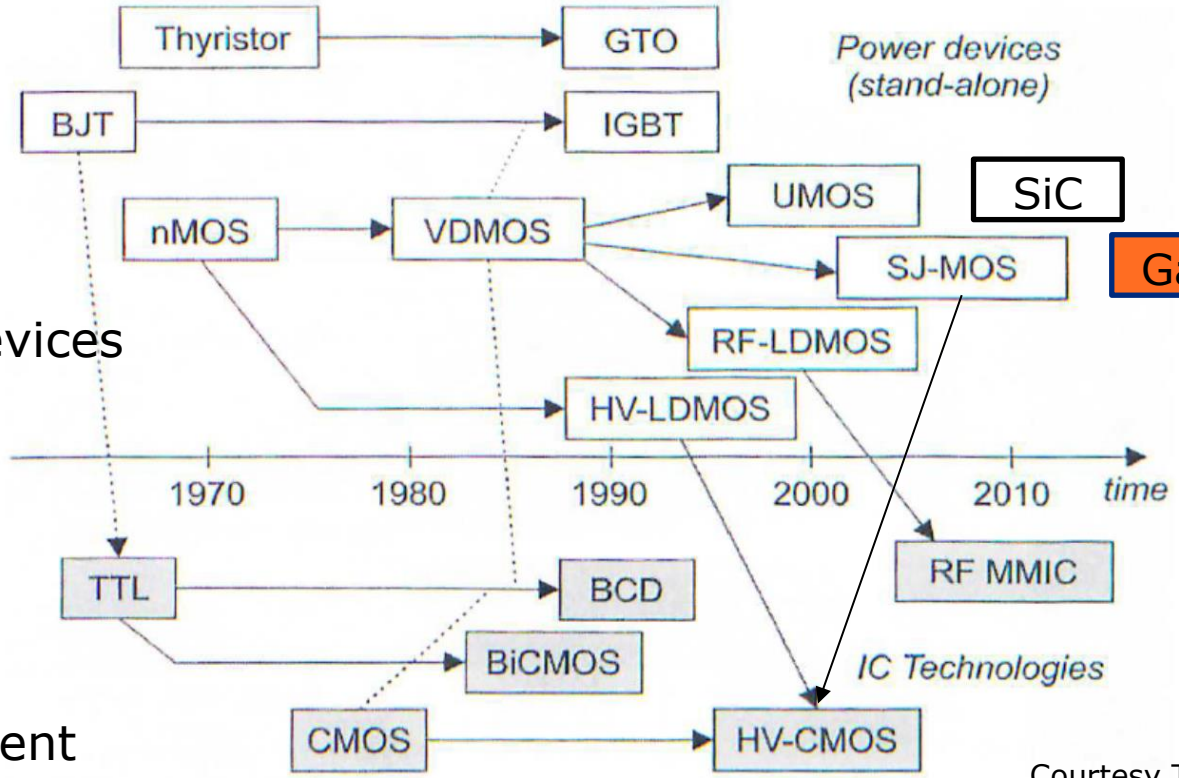
How to transfer the discrete GaN device into CMOS?

So far:

Silicon devices

into

silicon environment



new challenge:

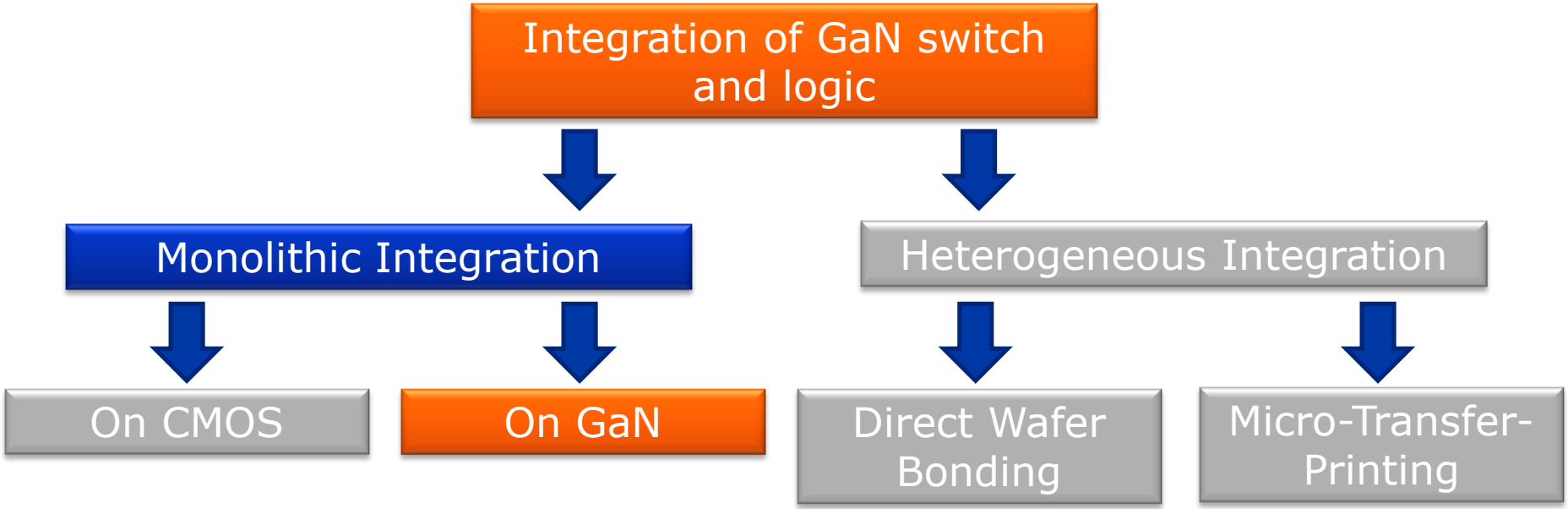
material mix

?

Courtesy T. Erlbacher: Lateral Power Transistors in Integrated Circuits

Monolithic Integration on GaN

Integration variants GaN and CMOS

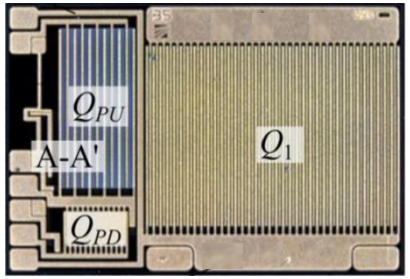


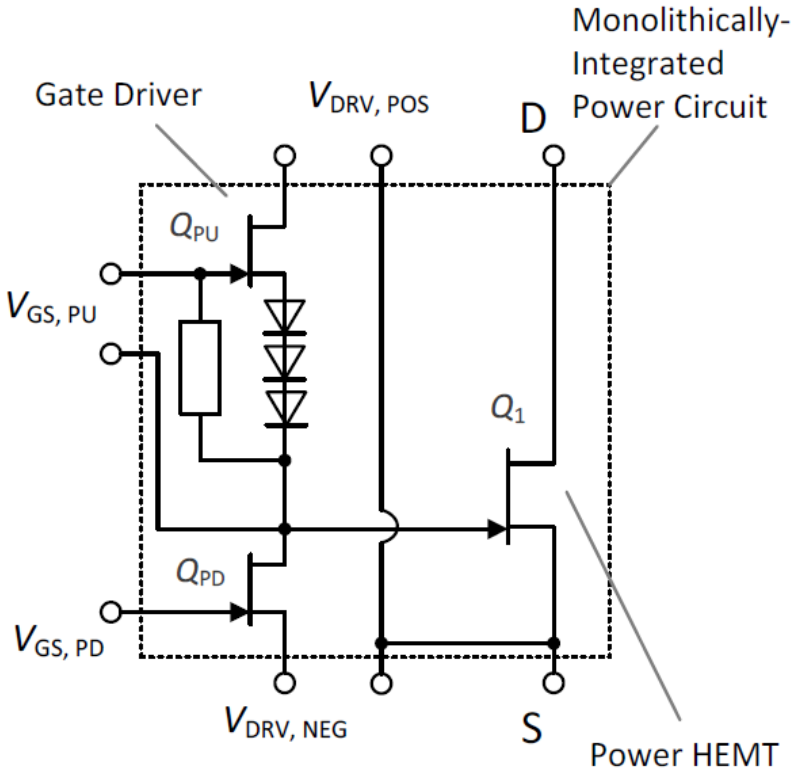
Monolithic Integration: pros & cons

- Advantages:
  - One chip, one substrate wafer, one process flow, one supplier
  - Reduction of assembly effort (less pick & place), reduced number of wire bonds (costs, inductance, signal delay & reliability!)
  - Reduced footprint
  - Lower costs especially on system level

R. Reiner, ISPS 2016

- Integration of push-pull type gate driver and D-mode power transistor
- Reduction of gate loop inductance and disturbances caused by drain-gate coupling => fast slew rates and stable switching



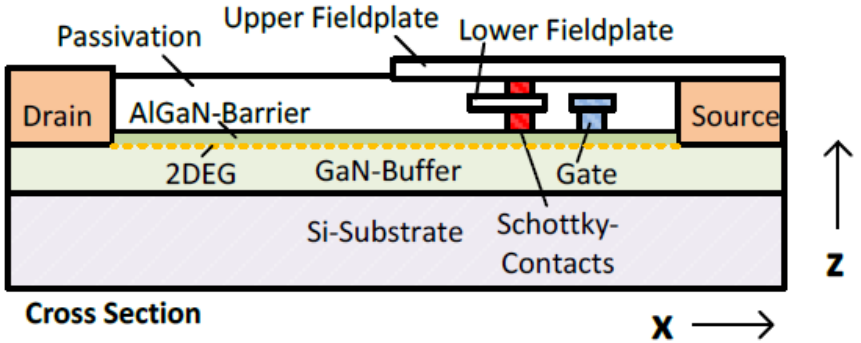


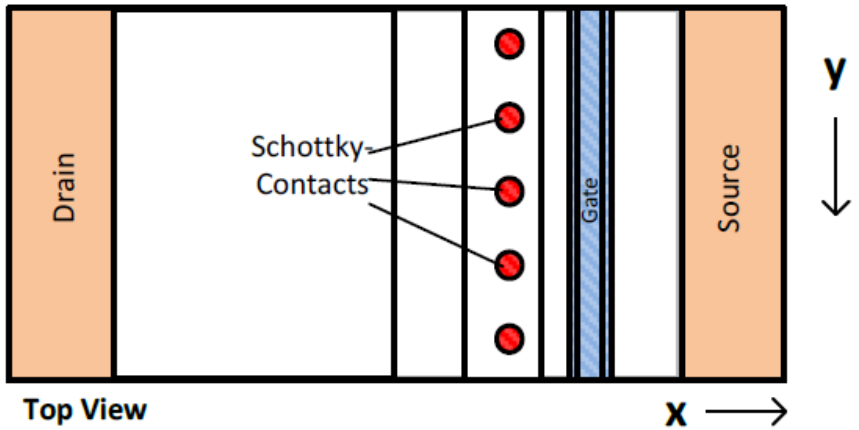
Richard Reiner et al., Monolithically-Integrated Power Circuits in High-Voltage GaN-on-Si Heterojunction Technology; 13th International Seminar on Power Semiconductors, Prague, 2016S.

Stefan Mönch et al., in Proc. WiPDA 2015, pp.: 92-97, Nov. 2015

R. Reiner, ISPS 2016

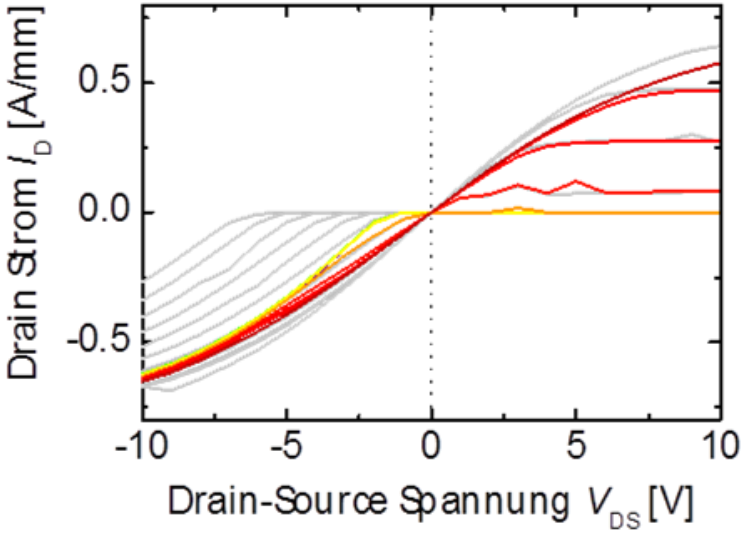
- Integration of Free-Wheeling Diode (FWD)
- HEMT without body diode
- External diode increases reverse-recovery charge and additional parasitics

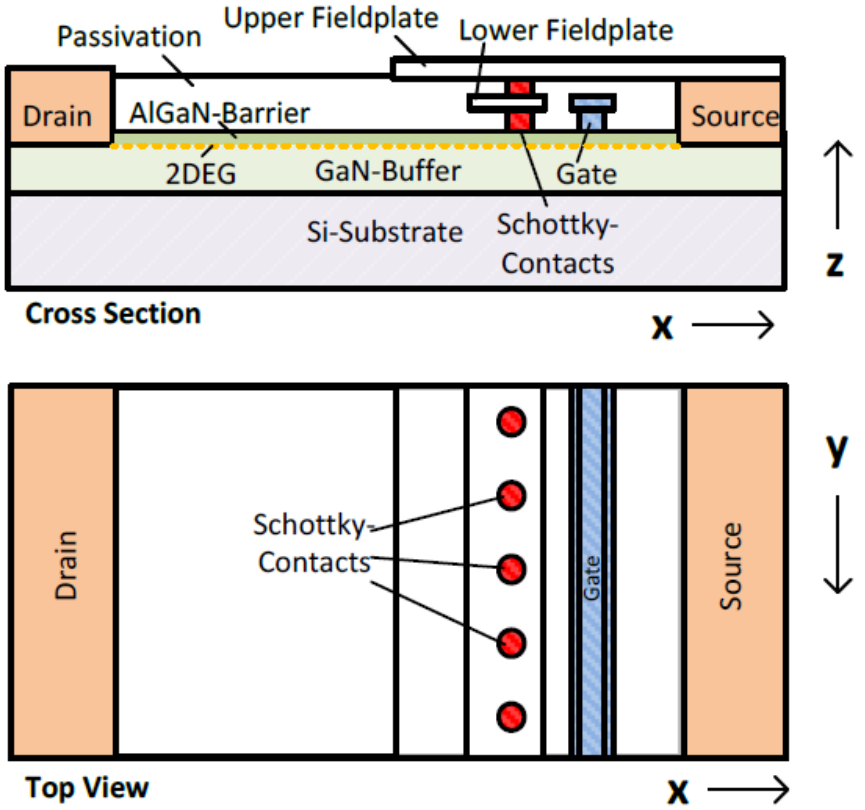




Richard Reiner et al., Monolithically-Integrated Power Circuits in High-Voltage GaN-on-Si Heterojunction Technology; 13th International Seminar on Power Semiconductors, Prague, 2016

R. Reiner, ISPS 2016

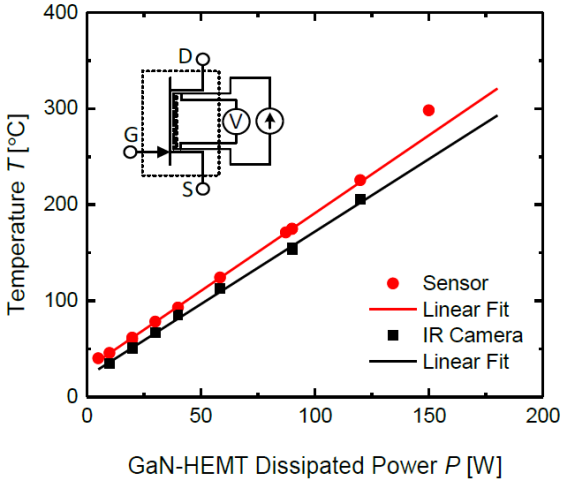


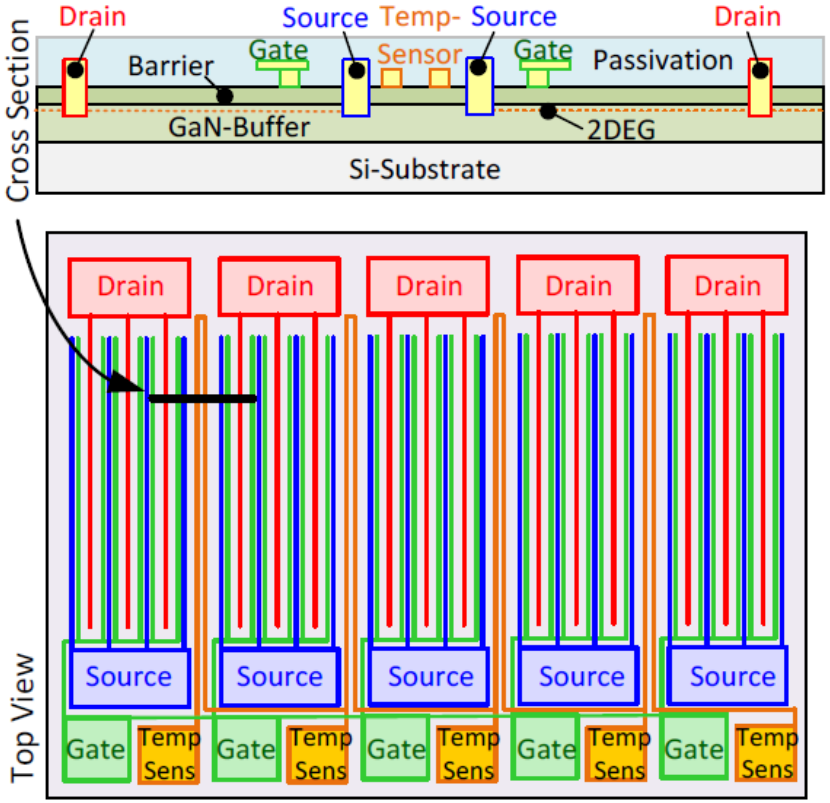


Richard Reiner et al., Monolithically-Integrated Power Circuits in High-Voltage GaN-on-Si Heterojunction Technology; 13th International Seminar on Power Semiconductors, Prague, 2016

R. Reiner, ISPS 2016

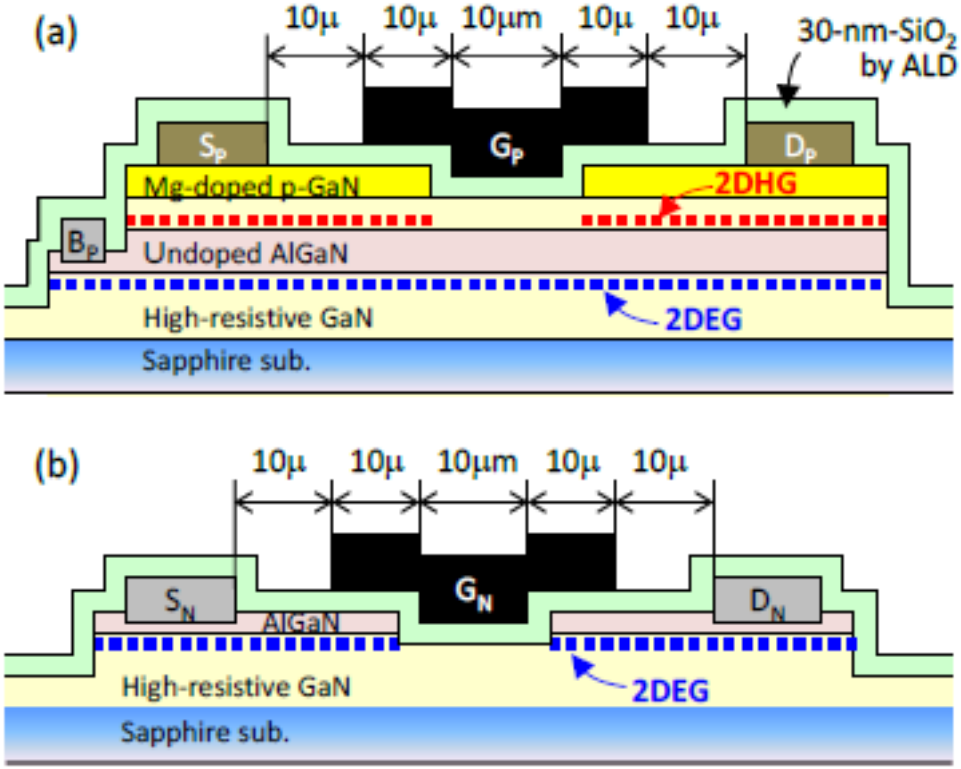
- Integration of temperature sensor
- Metal meander





A. Nakajima, ISPS 2016

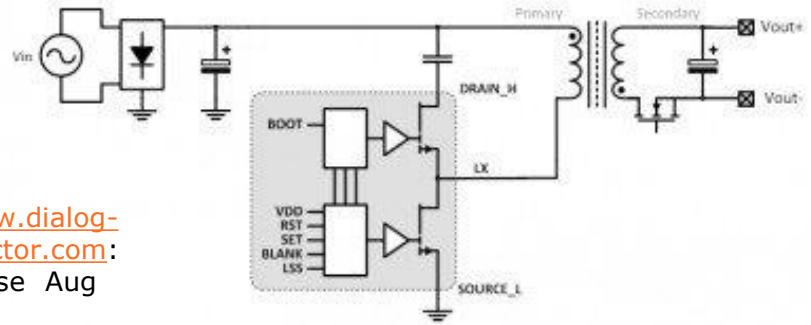
- Integration of LV N-channel and p-channel into 600V HEMT process

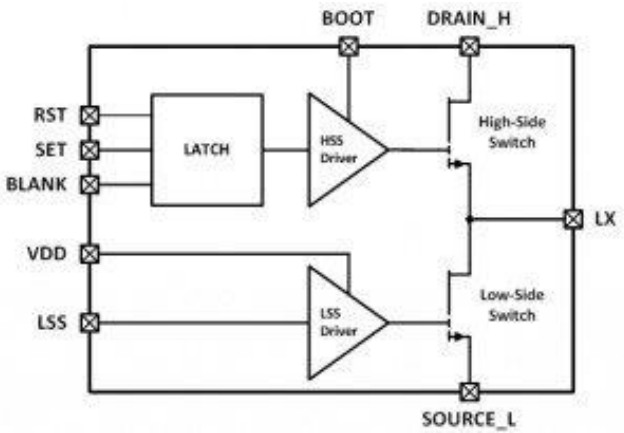


Akira Nakajima et al.; Monolithic Integration of GaN-based Normally-off P- and N-channel MOSFETs; 13th International Seminar on Power Semiconductors, Prague, 2016

DA8801 anouncement by Dialog

- SmartGan™ DA8801 providing monolithic integration of GaN power FETS together with analog drivers and logic
- GaN power IC product …, using TSMC's 650 Volt GaN-on-Silicon process technology
- Dialog's DA8801 half-bridge integrates building blocks, such as gate drives and level shifting circuits, with 650V power switches … with up to 94 percent power efficiency.

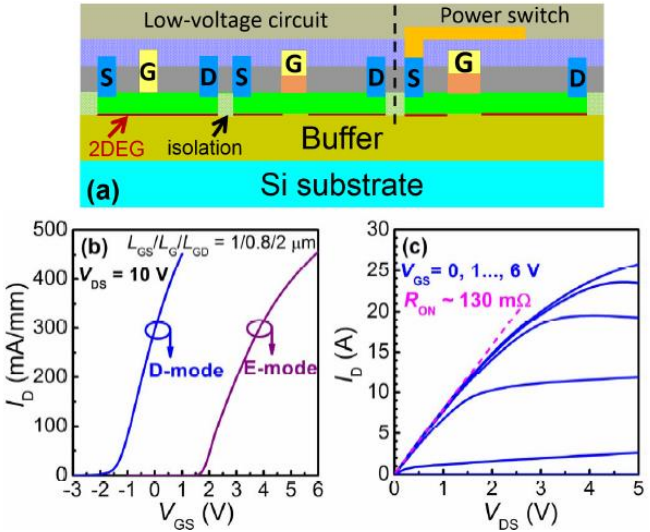


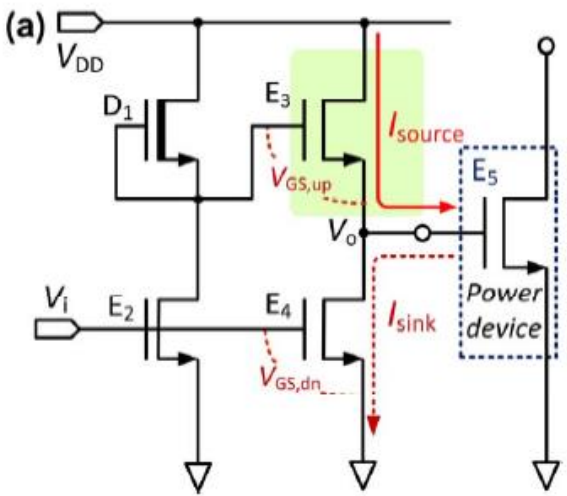


https://www.dialog-semiconductor.com: press-release Aug 25 2018

Tang et al, ISPSD 18

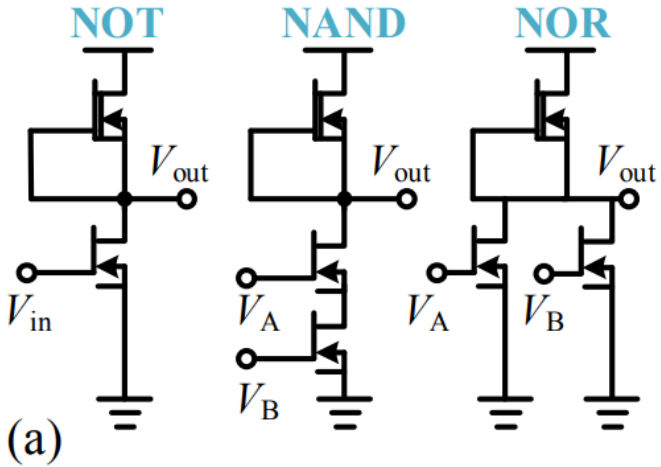
- E-mode GaN power switch and GaN based gate driver
  - LV E/D mode HEMTs with L_G=0.8μm; L_{GS}=1μm and L_{GD}=2μm

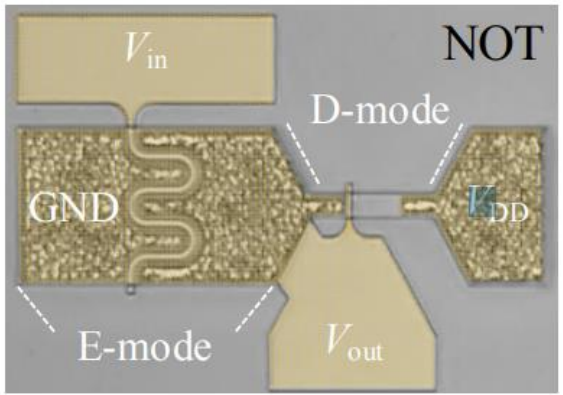


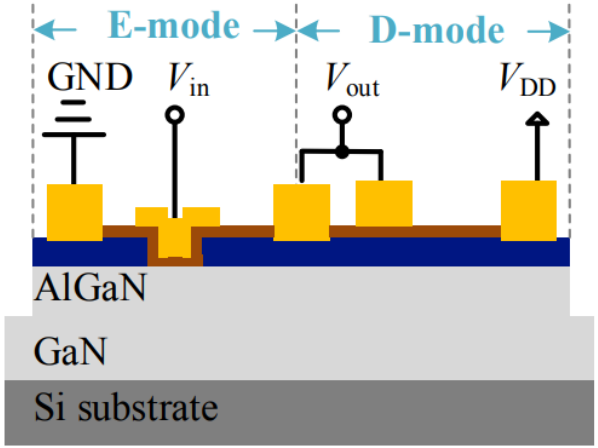


Gaofei Tang et al., High-Speed, High Reliability GaN Power Device with Integrated Gate Driver; 30th International Symposium Seminar on Power Semiconductor Devices and ICs, Chicago, 2018

Zhu & Matioli, ISPSD 18

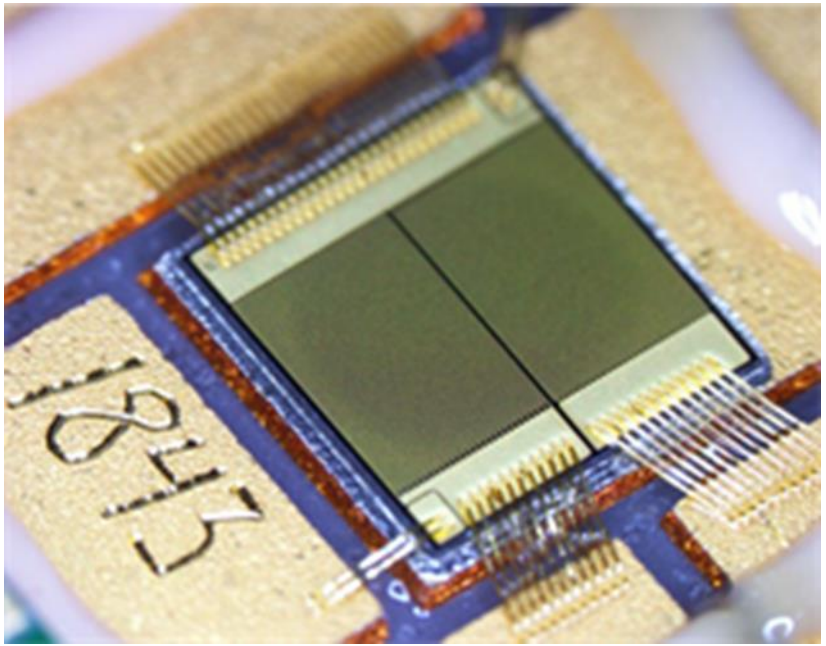


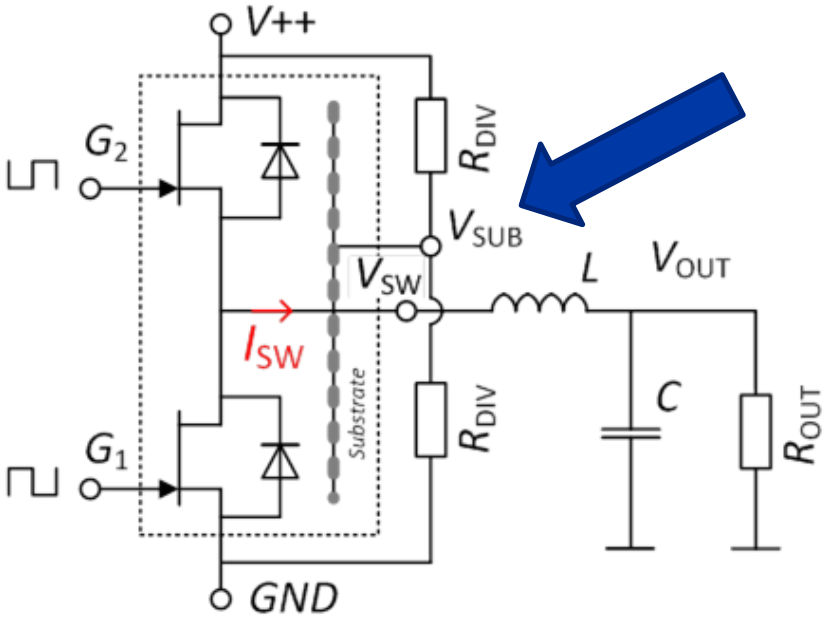




Minghua Zhu and Elison Matioli, Monolithic Integration of GaN-Based NMOS Digital Logic Gate Circuits with E-Mode Power GaN MOSHEMTs; 30th International Symposium Seminar on Power Semiconductor Devices and ICs, Chicago, 2018

IAF: Monolithic Half-Bridge



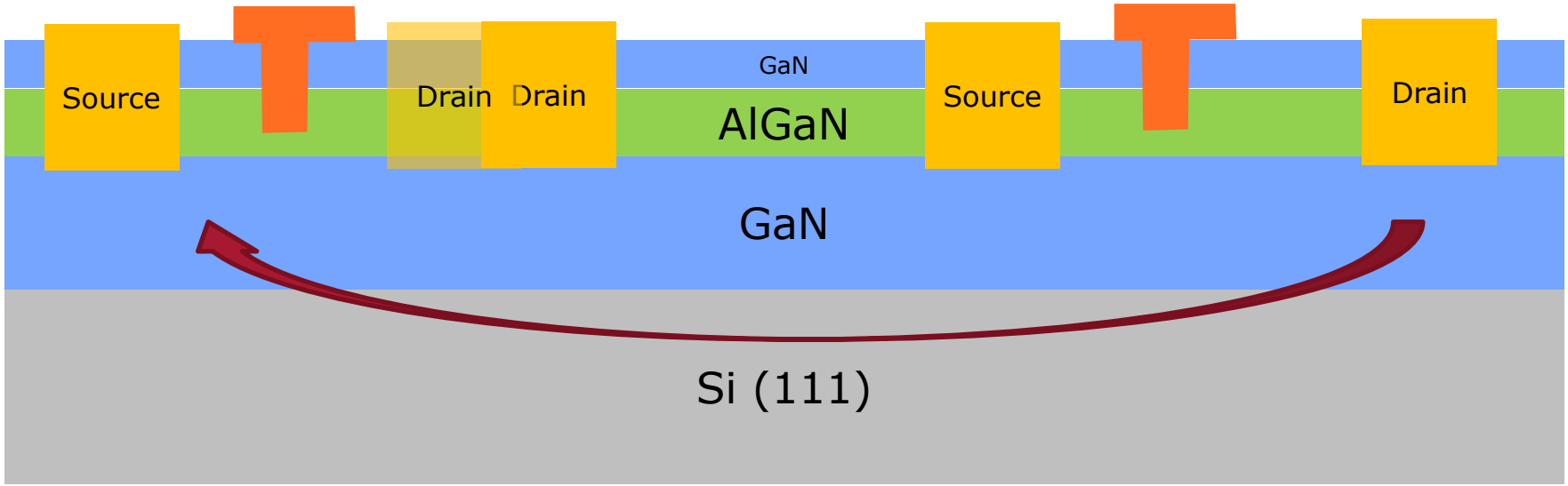


B. Weiss et al., Soft-switching 3 MHz converter based on monolithically integrated half-bridge GaN-chipin Proc. WiPDA 2016

Isolating issue

- Low side or LV

high side or HV

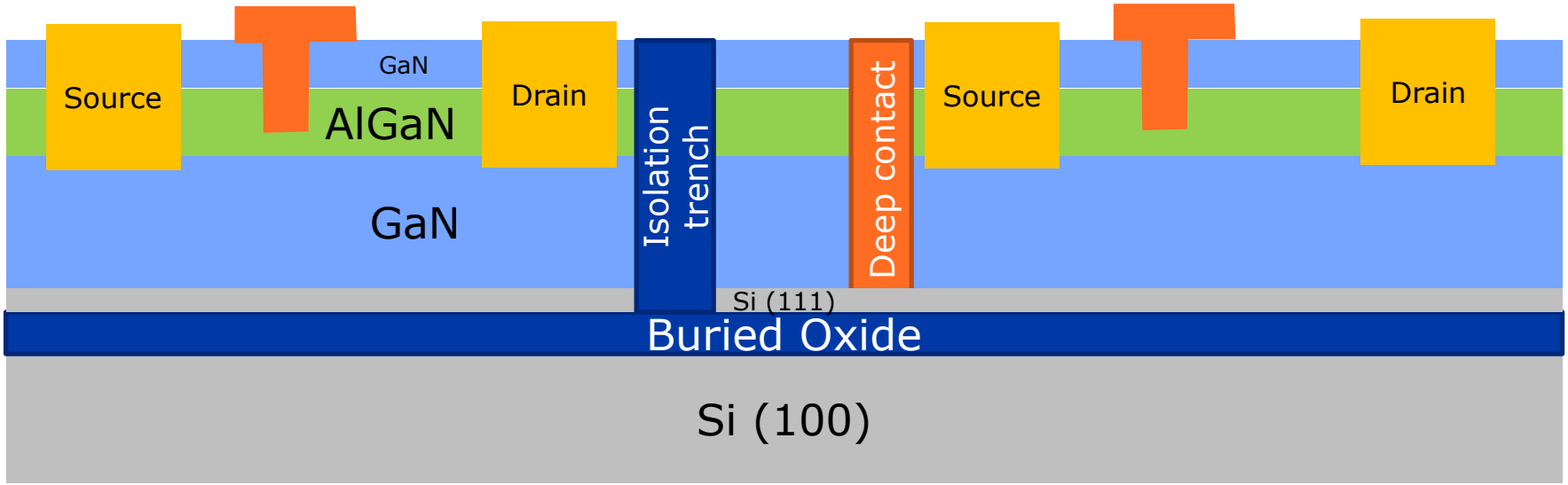


- Common conductive silicon substrate: single potential at a time

Isolating issue solved by SOI substrate

- Low side

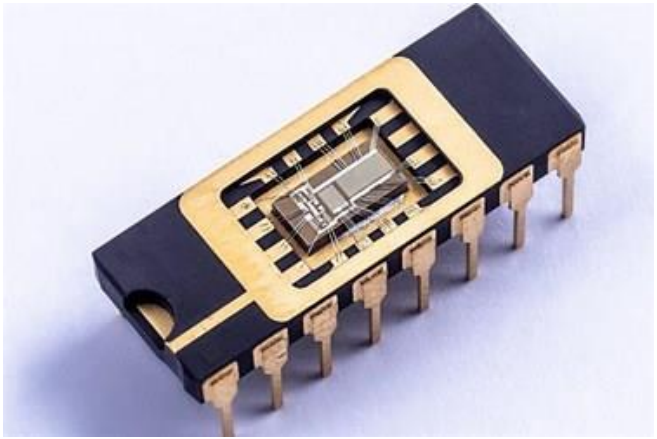
high side



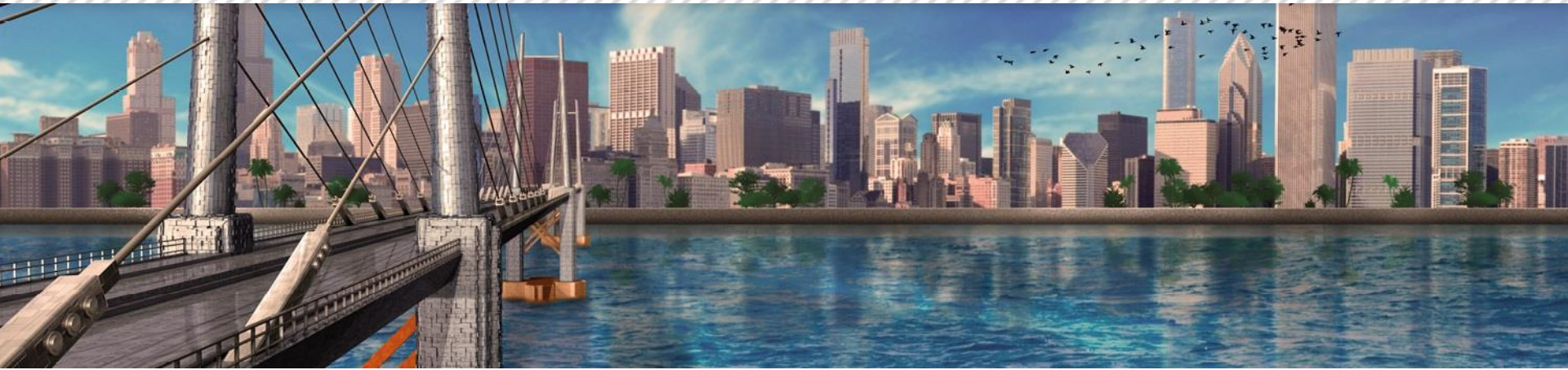
Karen Geens et al.; The Monolithic Integration Of GaN; Compound Semiconductor; Volume 23 Issue 6 August / September 2017

GaN half-bridge monolithically integrated with drivers

- converts an input voltage of 48V to an output voltage of 1V, with a pulse width modulation signal of 1 MHz
- half-bridge and drivers in one GaN-IC chip. Complemented by low voltage logic transistors, low- and high-ohmic resistors, MIM-capacitor,
- GaN-on-SOI and GaN-on-QST technology platforms that allow for a galvanic isolation of the power devices, drivers and control logic, by the buried oxide and oxide-filled deep trench isolation

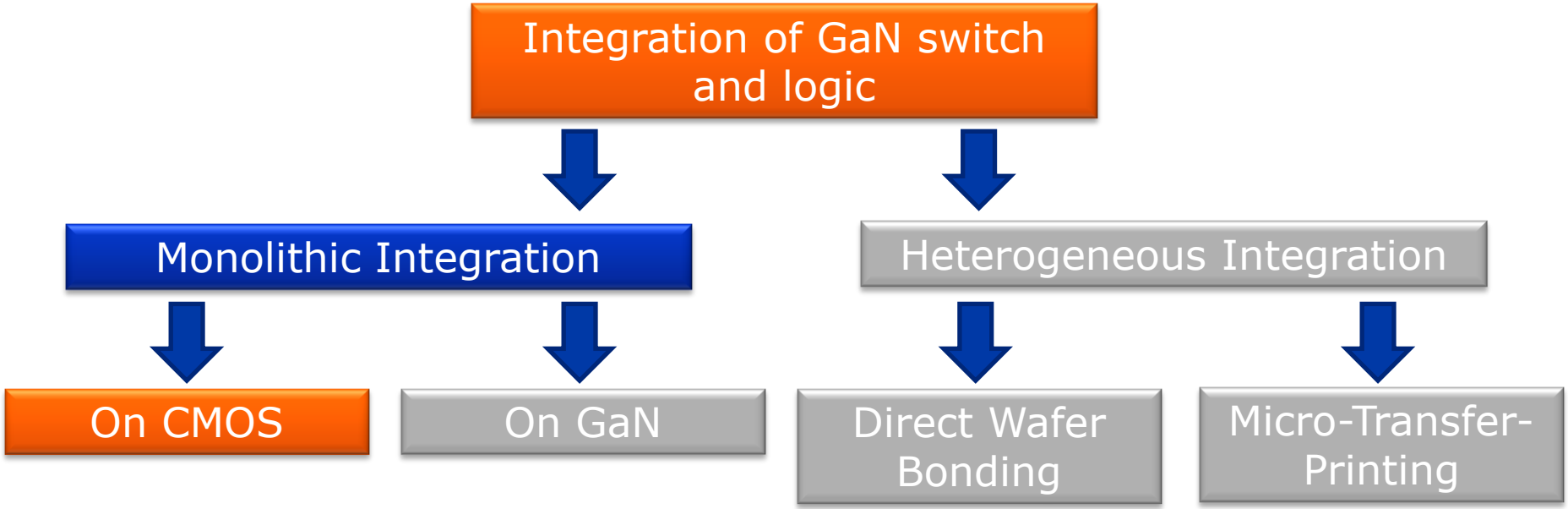


http://www.newelectronics.co.uk/electronics-news/imec-demonstrates-fully-monolithical-co-integration-of-gan-half-bridge-with-drivers/214992/



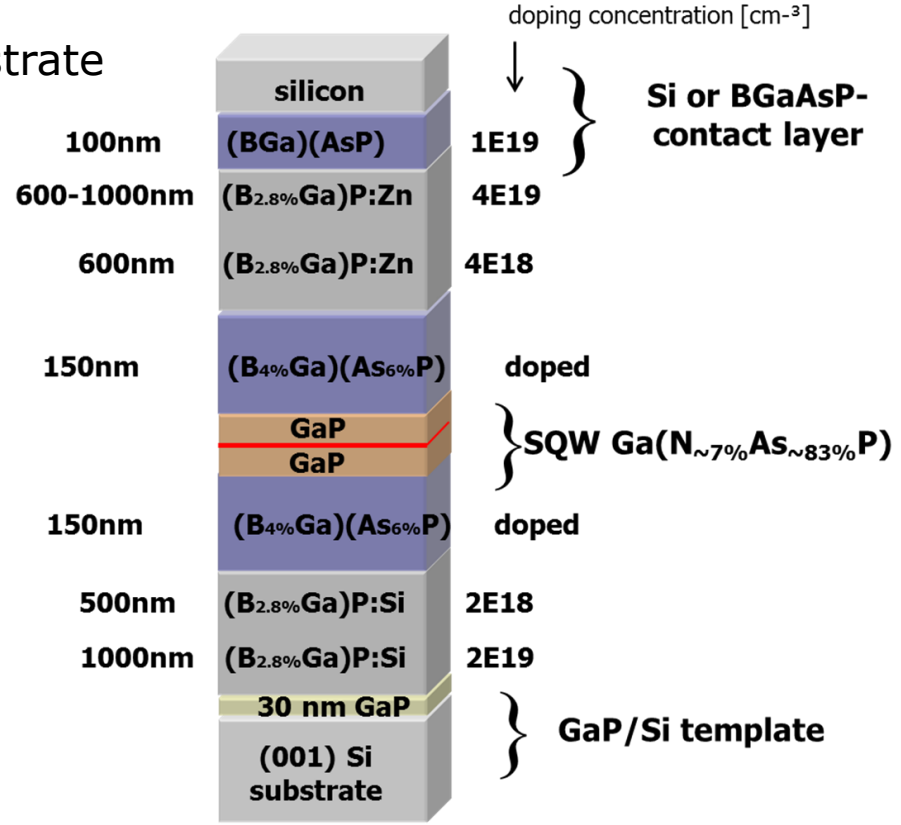
Monolithic integration on Si CMOS

Integration variants GaN and CMOS



Schematic of III/V based LED

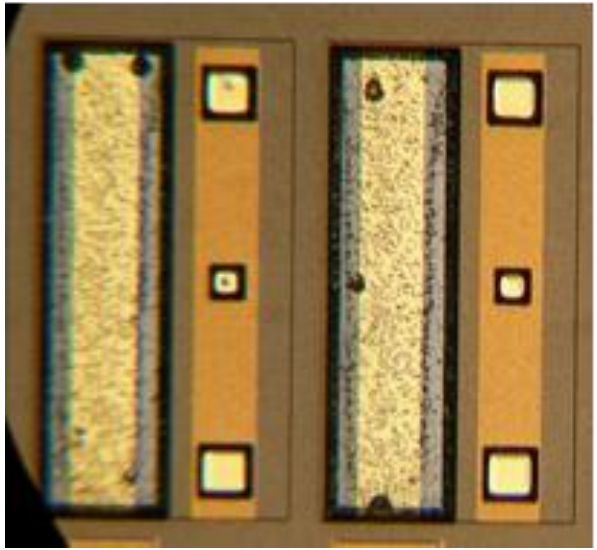
- FEOL processed CMOS wafer as substrate
- X-FAB processing until ILD
- MOVPE at NAsP
- Metal at NAsP
- Main interface: GaP on (001) Si

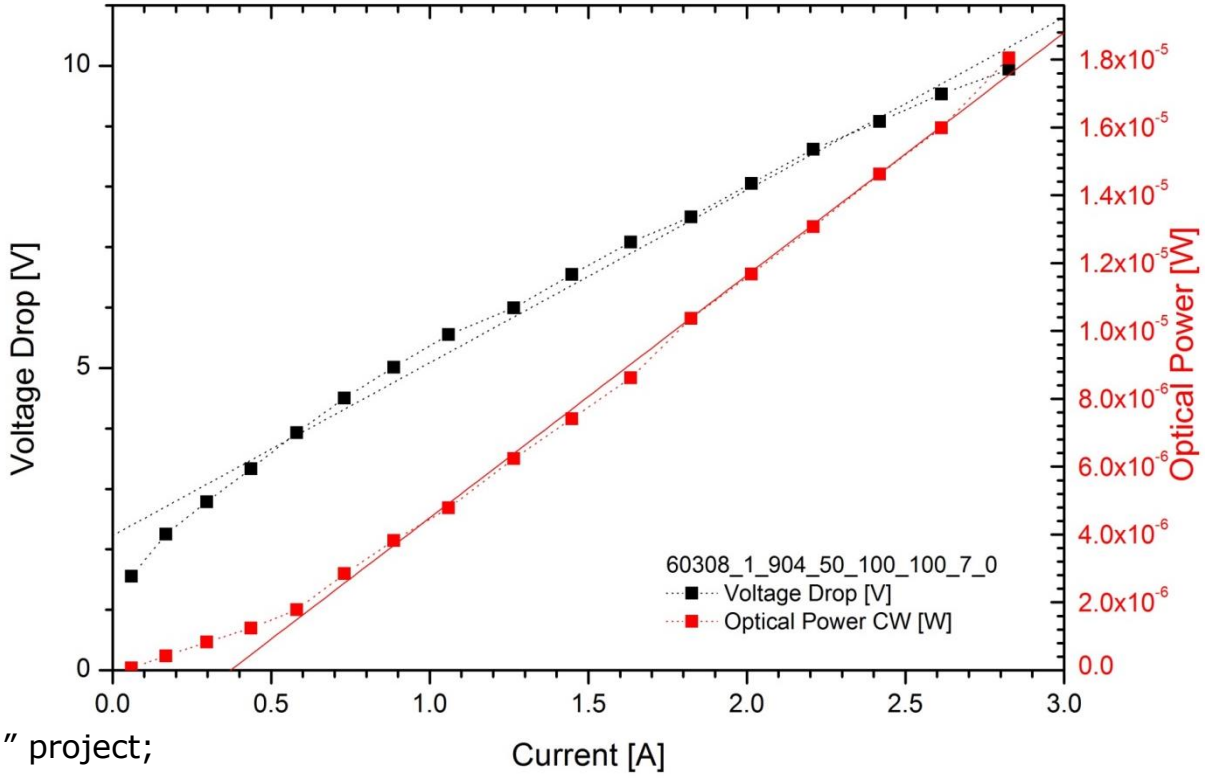


Sketch by NAsP III/V GmbH, "Modelan" project; 16N12068

GaN based LED

- Working LED

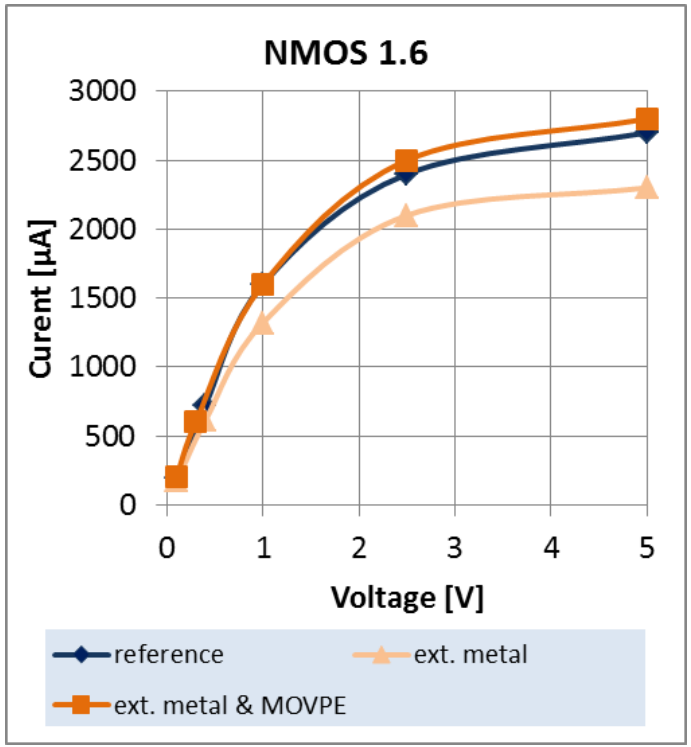




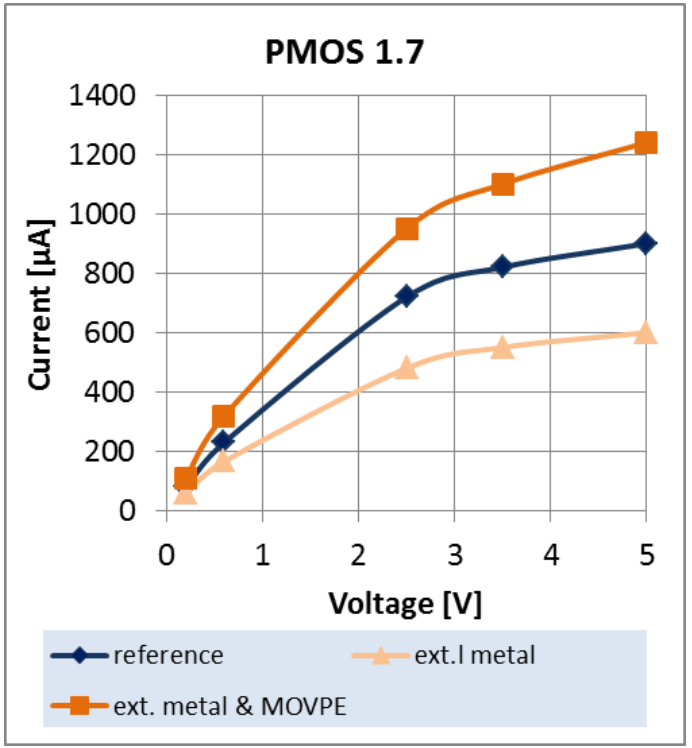
Results by NAsP III/V GmbH, “Modelan” project; 16N12068

CMOS performance

- Significant disturbance, nevertheless working CMOS transistors etc.

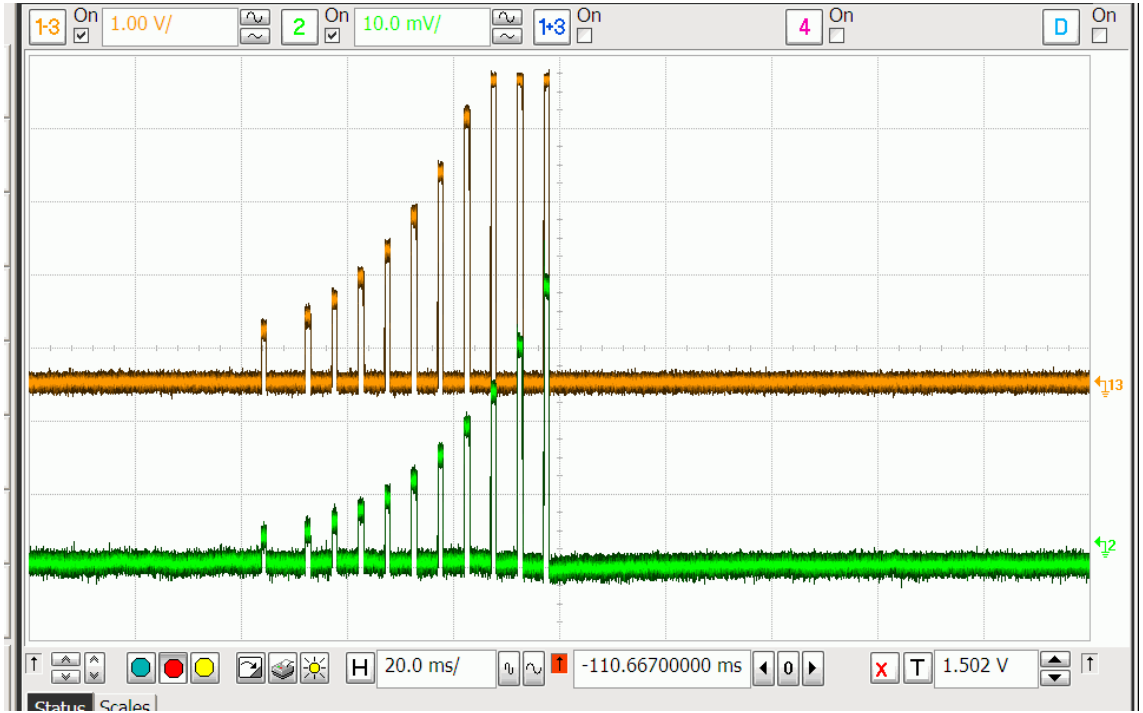


Vgs=5V



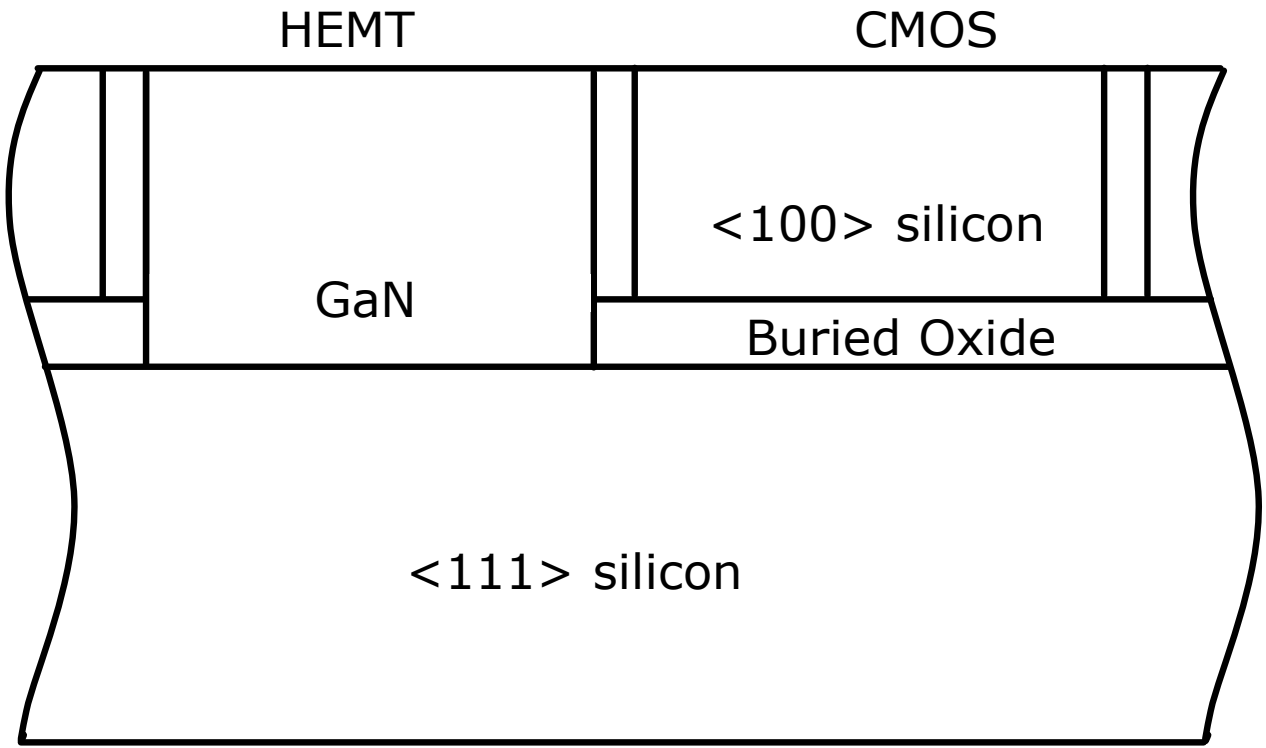
Optical coupling

- Working opto coupler:
- 4V input
- 25mV output



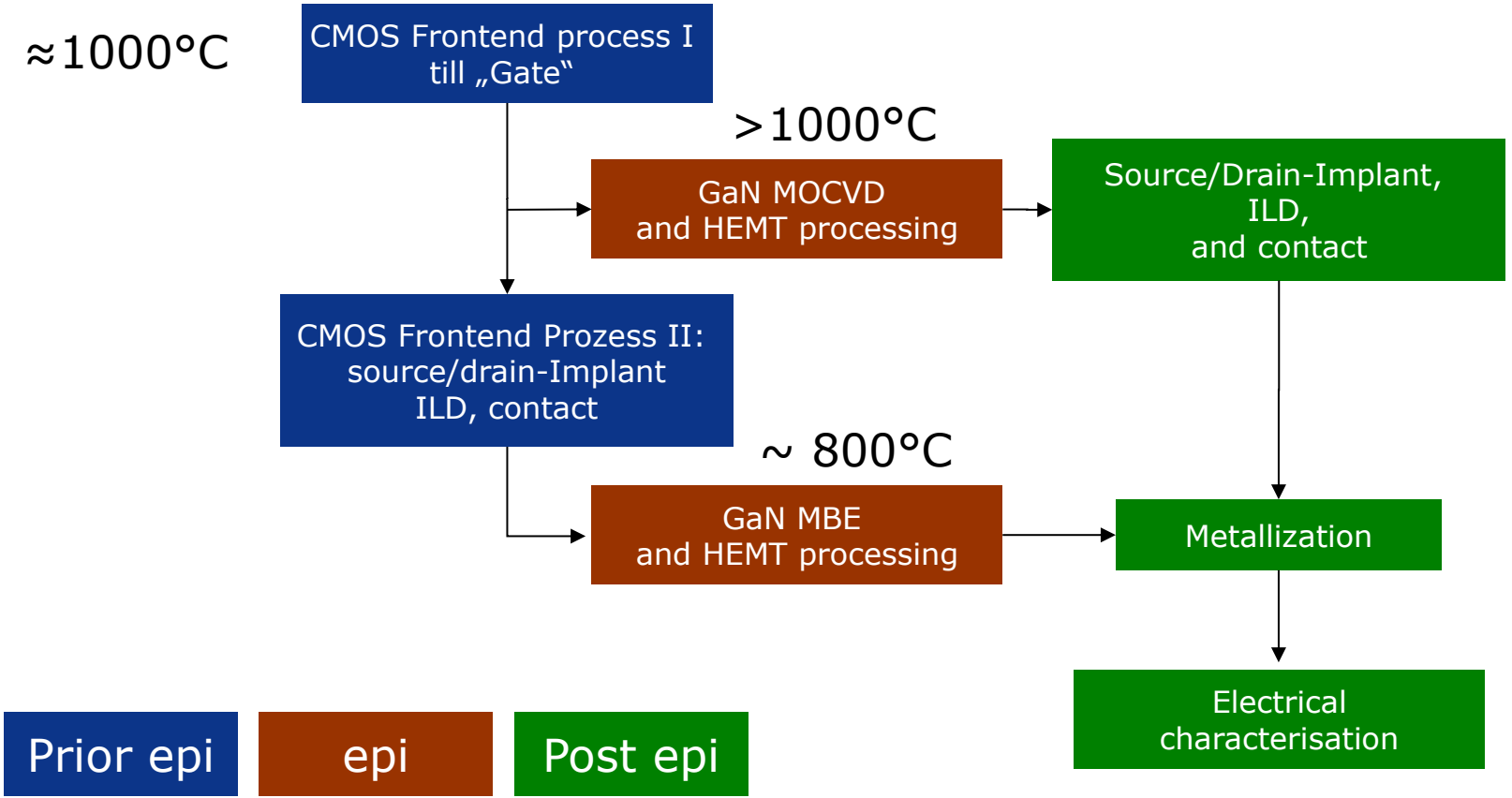
Results by NAsP III/V GmbH, “Modelan” project; 16N12068

US 8759169 B2 with SOI wafer

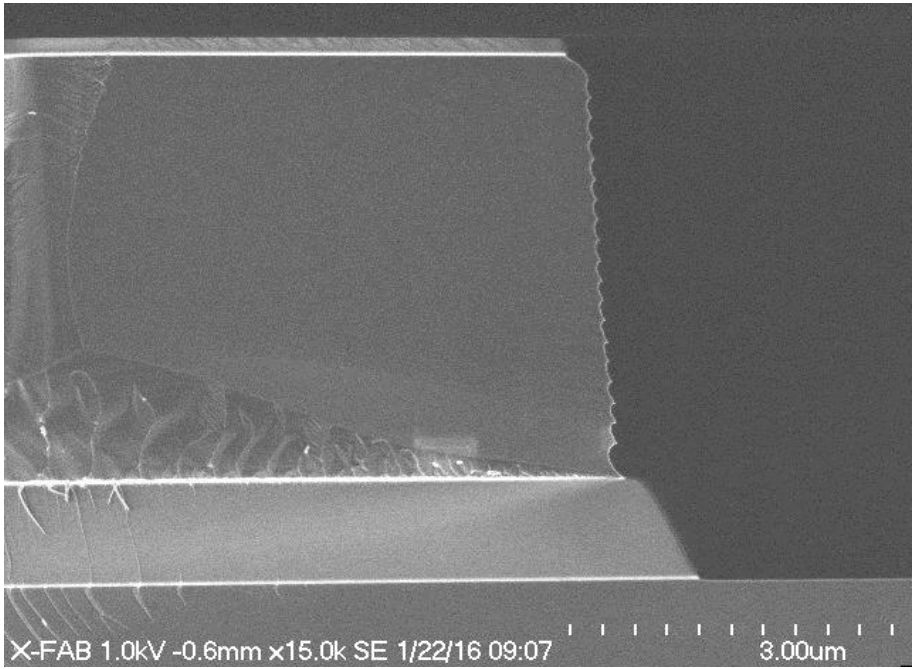


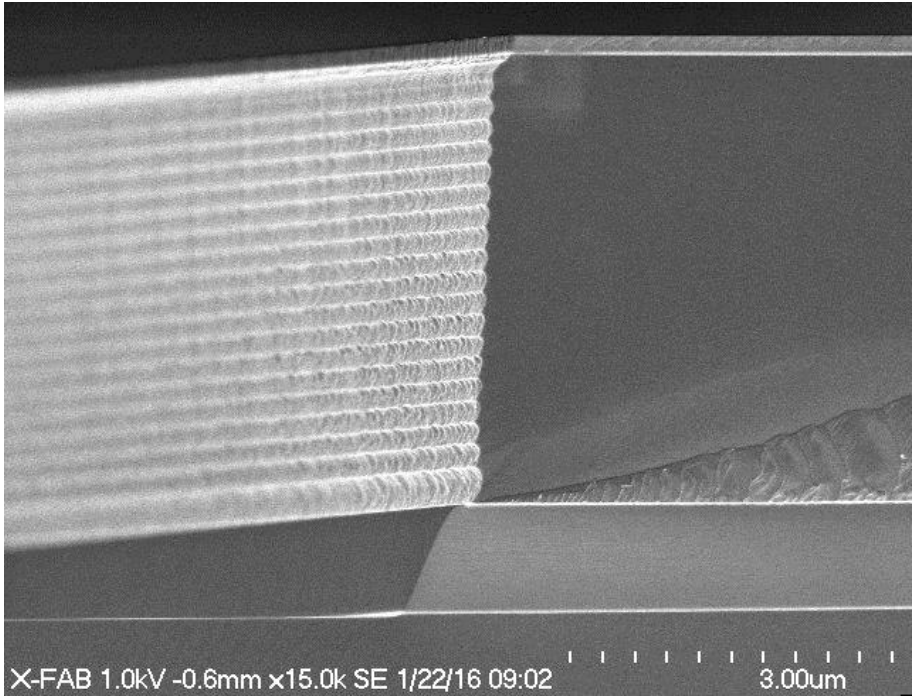
Priority data Oct 31. 2009 DE 10 2009 051 520 by Kittler & Lerner

Basic options / restrictions for flow



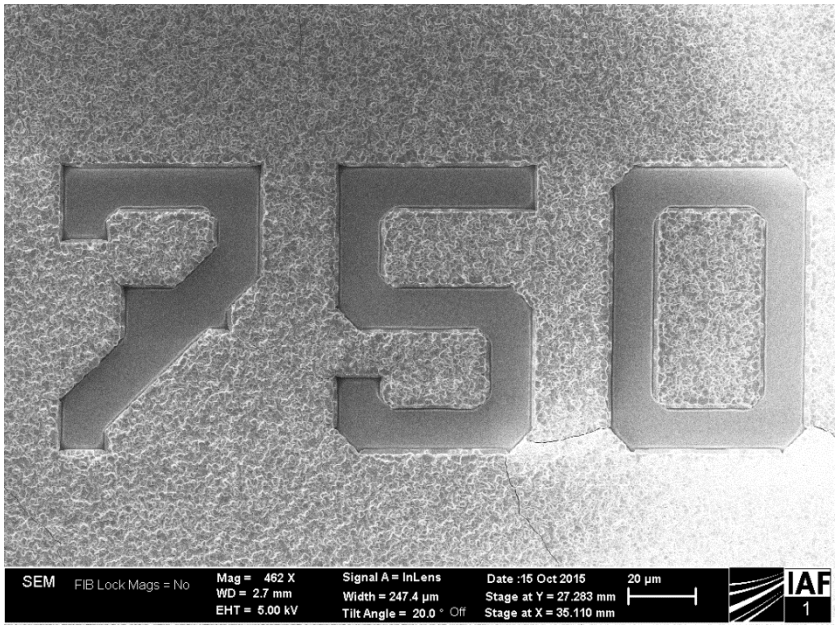
Etched SOI wafers





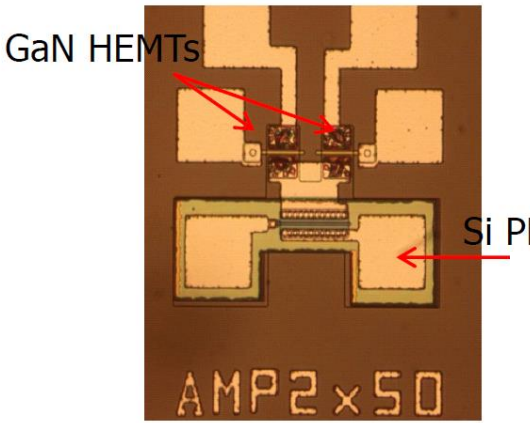
Epitaxy

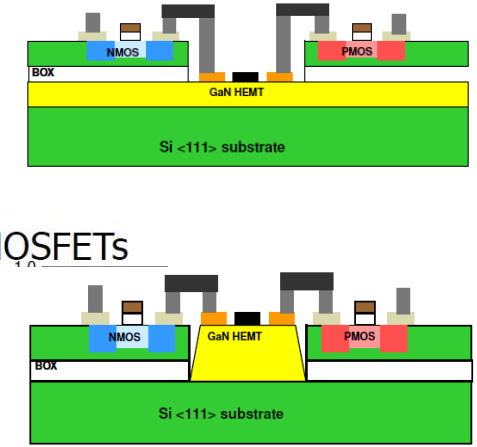
- Good epi quality in SOI tub
- Non-selective growth, poly crystalline GaN outside the tub
- Needs to be removed
- Additional material -> additional stress
- Open issue at the end of the project

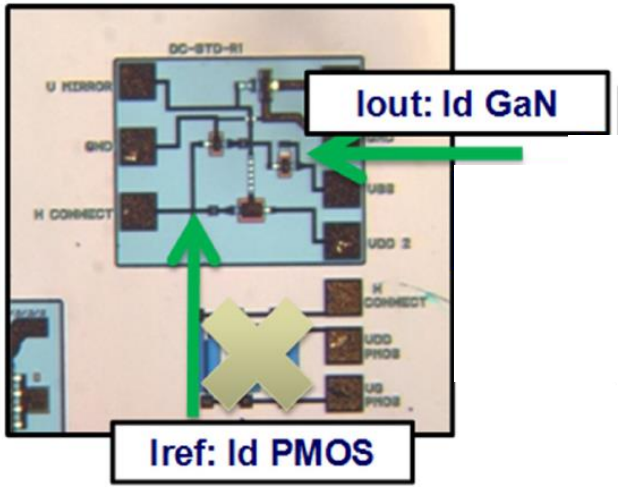


Publication Raytheon/MIT

- A quite similar approach has been published by Raytheon & MIT for
  - Current mirror: 0.25µm GaN HEMT + 1µm PMOS
  - GaN PA with CMOS PWM







T. E. Kazior, R. Chelakara, W. Hoke, J. Bettencourt, T. Palacios, H. S. Lee, *"High Performance Mixed Signal and RF Circuits Enabled by the Direct Monolithic Heterogeneous Integration of GaN HEMTs and Si CMOS on a Silicon Substrate"*, IEEE Symposium on Compound Semiconductor Integrated Circuit (CSICS), Oct 2011

T. E. Kazior, "Heterogeneous Integration of GaN and Si CMOS: A Path to "Smart" Electronics", Short Courses of the 26th International Symposium on Power Semiconductor Devices & ICs, Waikoloa, June 2014

Epi growth: MBE versus MOCVD

- MIT / Raytheon did the GaN epitaxy with Molecular Beam Epitaxy, MBE
- Advantage of MBE: lower epi temperature than Metal Organic Chemical Vapour Deposition, MOCVD
  - Less disturbance of CMOS, CMOS first possible
- But MBE with lower growth rates (= lower throughput) than MOCVD
- Mass production (at acceptable throughput) probably only with MOCVD

- Especially due to epi growth a monolithic process gets very complex and difficult

IBM, MIT, Veeco and Columbia University

- Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) fabricated on 200mm-diameter silicon-on-insulator (SOI) substrates with multiple crystal orientations

Hybrid-oriented SOI substrate with top Si (100) and bottom Si (111) preparation for MOCVD growth:

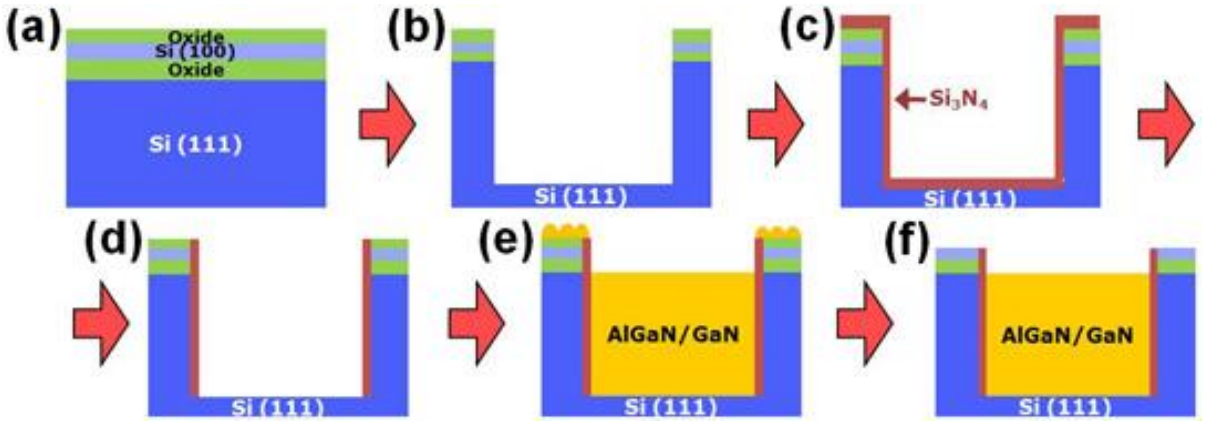
(a) CVD-SiO2 growth,

(b) dry etching to expose Si (111) plane,

(c) Si3N4 growth via CVD as isolation and diffusion barrier, (d) Si3N4 removal via dry etch to expose Si (111) plane,

(e) AlGaN/GaN HEMT growth,

(f) CVD-SiO2 removal via chemical-mechanical planarization.



Ko-Tao Lee, et al, IEEE Electron Device Letters, published online 27 June 2017

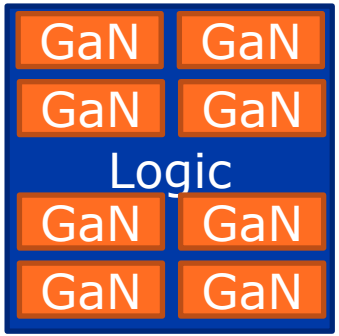
Monolithic Integration: pros & cons

- Advantages:
  - One chip, one substrate wafer, one process flow, one supplier
  - Reduction of assembly effort (less pick & place), reduced number of wire bonds (costs, inductance, signal delay & reliability!)
  - Reduced footprint
  - Lower costs especially on system level

- Drawbacks
  - Complex process (crystal orientation, thermal budget, thermal stability) or limited primitives
  - Mixed materials monolithic integration: contamination, mechanical and optical parameters
  - Partitioning versus current trade-off

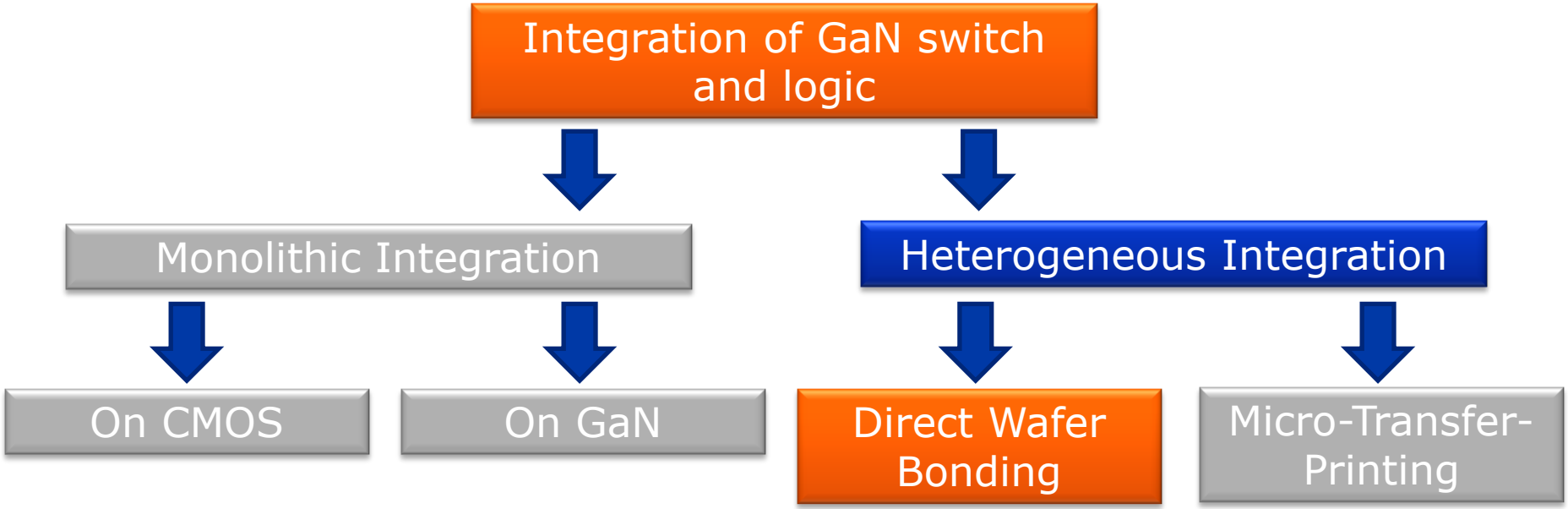
Partitioning problem in monolithic integration

- Expensive processing steps that become operative only in small parts of the IC
- Example: GaN epitaxial growth
  - In a pure GaN process the GaN epi-layer is used on the whole wafer
  - In a monolithic IC only a (small) part of the IC (of the wafer) has GaN ➪ higher costs per mm²
- A CMOS IC with integrated GaN should have an area partitioning closer to 50/50 than 99/1
  - But GaN HEMTs deliver ~6A/mm²
  - Thick CMOS Al metal with 6A/mm
  - Deep sub micron logic with X00µm wide metal …
  - ➪ thick copper RDL

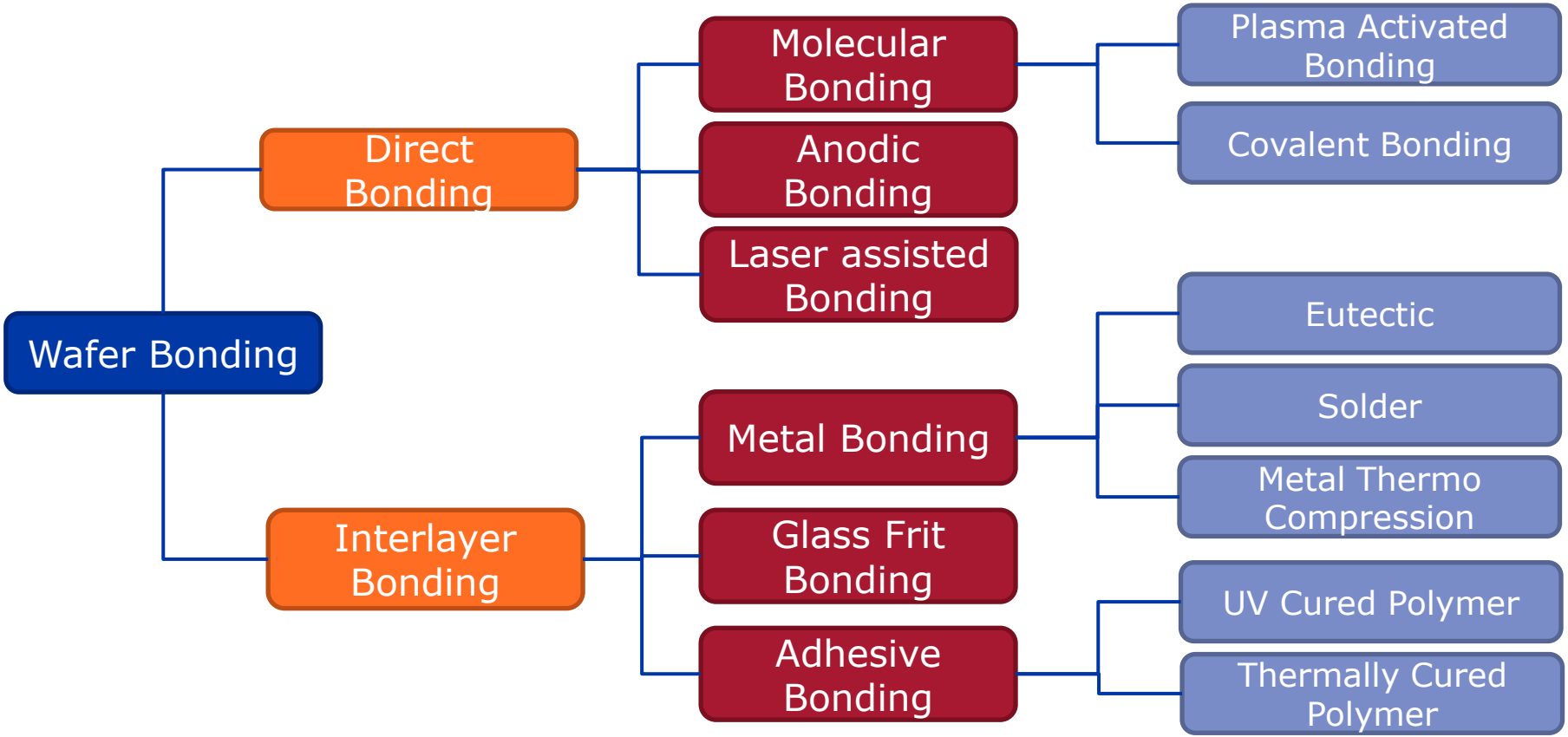


Heterogeneous integration by direct wafer bonding

Integration variants GaN and CMOS



Wafer bonding processes



Direct wafer bonding advantage

- Integration of non-lattice matched semiconductors
- Integration of semiconductors with different crystal structure
- Misfit dislocations only close to bond interface
- Direct bonding = no additional intermediate layers

- Two or more wafers can be integrated
- Each wafer (each chip) manufactured in its optimized process

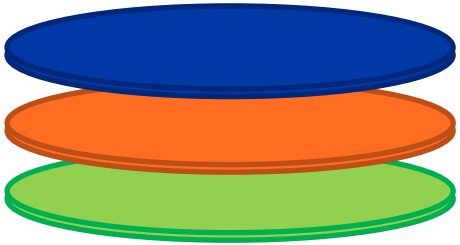
Different bonding approaches

Wafer to Wafer bonding

Bonding

Dicing

Pre-processed wafers



Chip to Wafer bonding

Bonding
Dicing

Dicing

Dicing

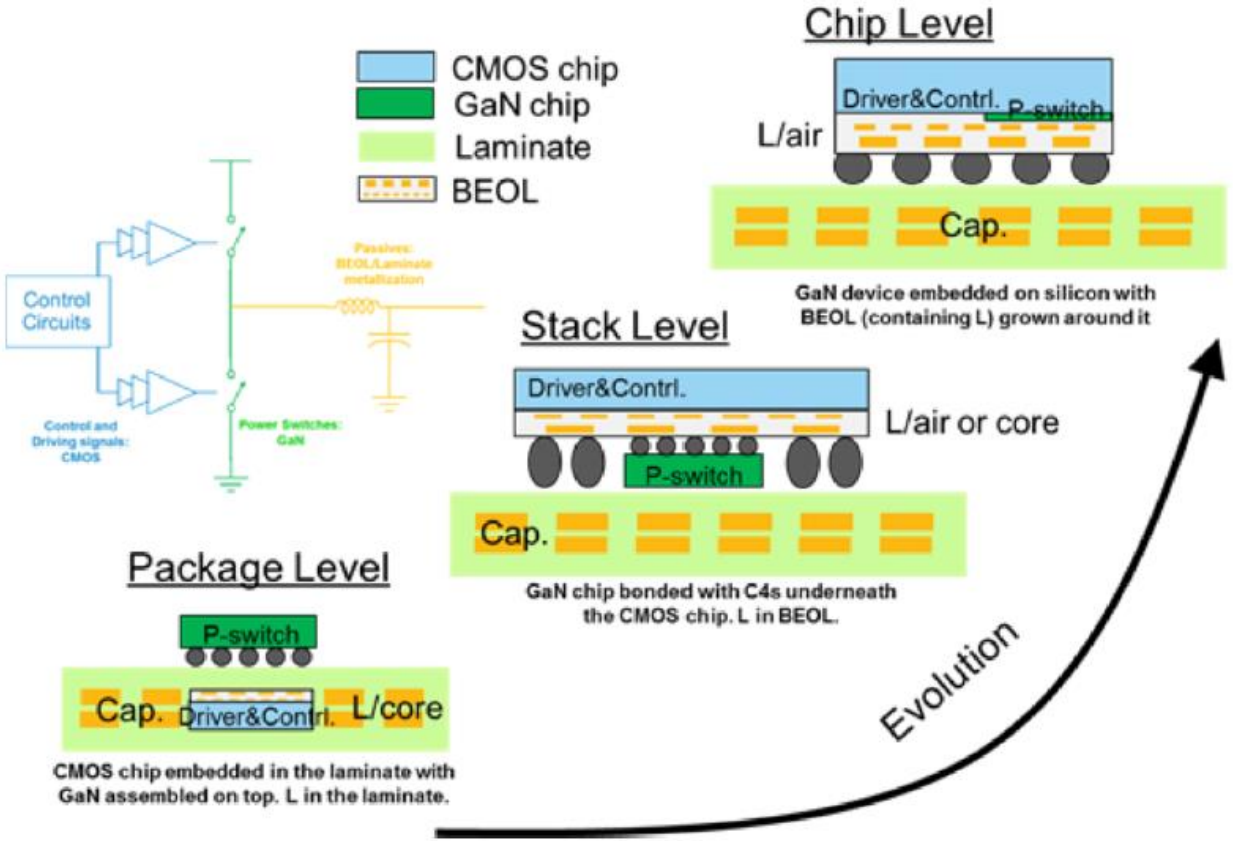
Chip to Chip bonding

Bonding

EU Horizon 2020 „GaNonCMOS“, partners

- University Leuven (Belgium)
- EpiGaN (Belgium)
- Fraunhofer IAF (Germany)
- IBM Research (Switzerland)
- AT&S (Austria)
- Tyndall National Institue (Ireland)
- Recom Engineering (Austria)
- PNO Innovation (Belgium)
- X-FAB (Germany)
- IHP Frankfurt(O) (Germany)

Different integration schemes



GaN-on-CMOS Integration by Direct Wafer Bonding, DWB

Direct wafer bonding:

- Deposit adhesive layers (typically oxides)
- Carefully clean the two surfaces
- Place the wafers in direct physical contact
- Anneal the wafer stack (300-500°C depending on adhesive layers)

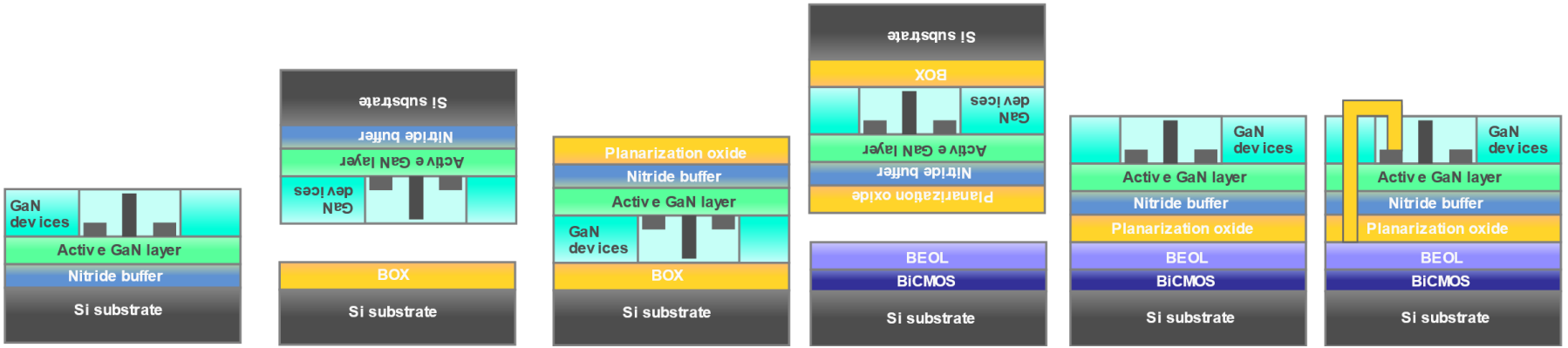
Two main schemes to integrate GaN on top of CMOS using DWB:

- Front-side bonding
- Back-side bonding

Courtesy of IBM, Zurich

GaN-on-CMOS Integration by DWB: Backside bonding

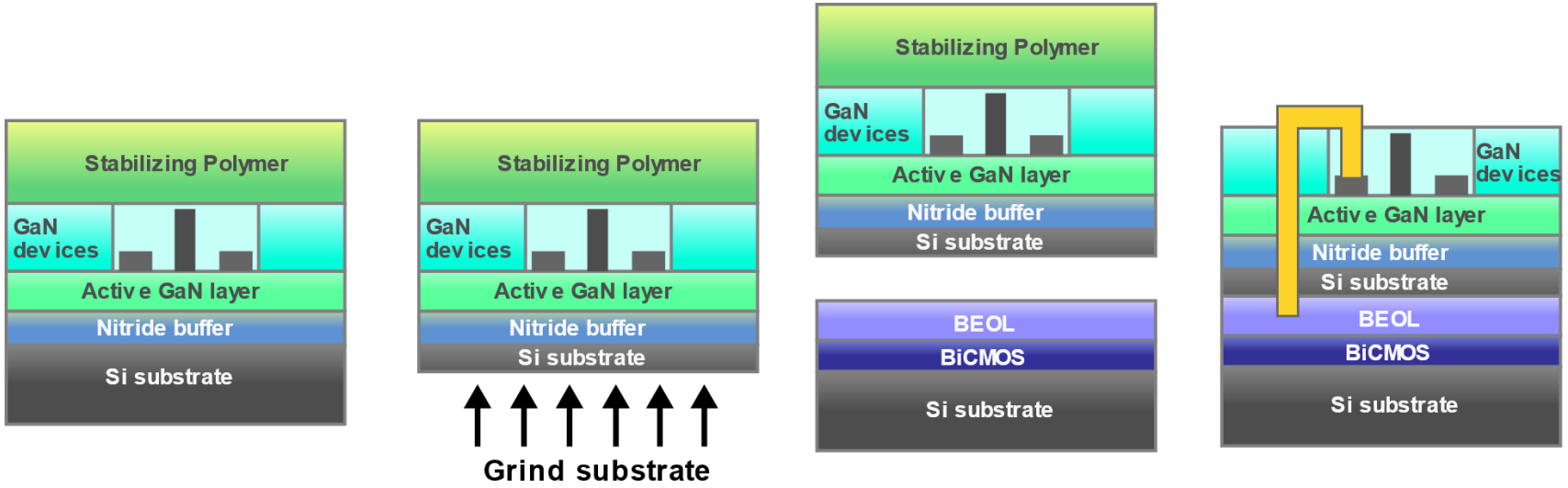
Step 1	Step 2	Steps 3 & 4	Step 5	Step 6	Step 7
1.1 Growth of GaN stack 1.2 Fabrication of GaN FETs 1.3 Planarization	2.1 Bonding oxide deposition 2.2 Surface cleaning 2.3 Direct wafer bonding to Si(100) transfer wafer	3.1 Si(111) substrate removal 4.1 Oxide deposition 4.2 Planarization by CMP	5.1 Planarization of BiCMOS 5.2 Direct wafer bonding to IHP BiCMOS wafer	6.1 Si(100) removal by Bosch etcher	7.1 Interconnect formation



Two DWB steps: Increases total bonding defects
Requires sub-1 nm surface topology at both DWB steps

Courtesy of IBM, Zurich

GaN-on-CMOS Integration by DWB: Frontside bonding

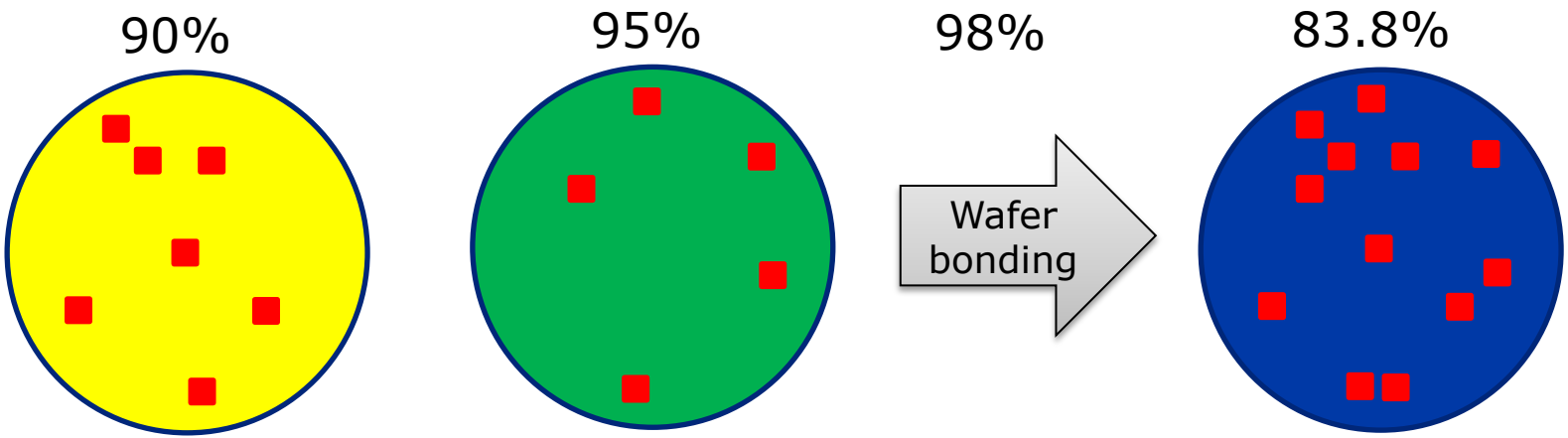


Reduces DWB steps to one, but requires a complex process to stabilize the wafer during the Si substrate thinning (3M Wafer Support System)

Courtesy of IBM, Zurich

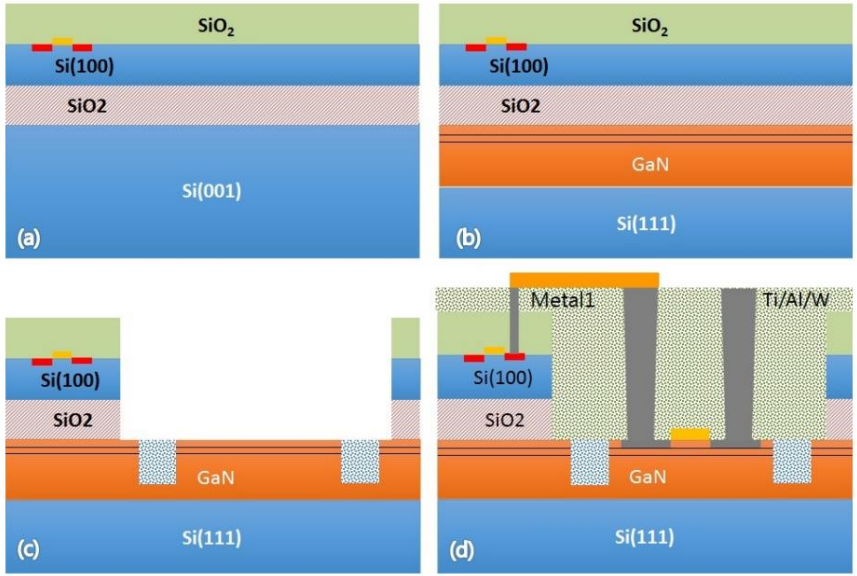
Direct Wafer Bonding

- Several challenges involved
  - Very flat, smooth and particle-free surface(s) necessary (thick metal topology!) <=> bonding defects
  - Wafer diameter and chip sizes should fit together => co-design of chips required
  - Alignment accuracy (on wafer level!)
  - Interconnects
- Yield?

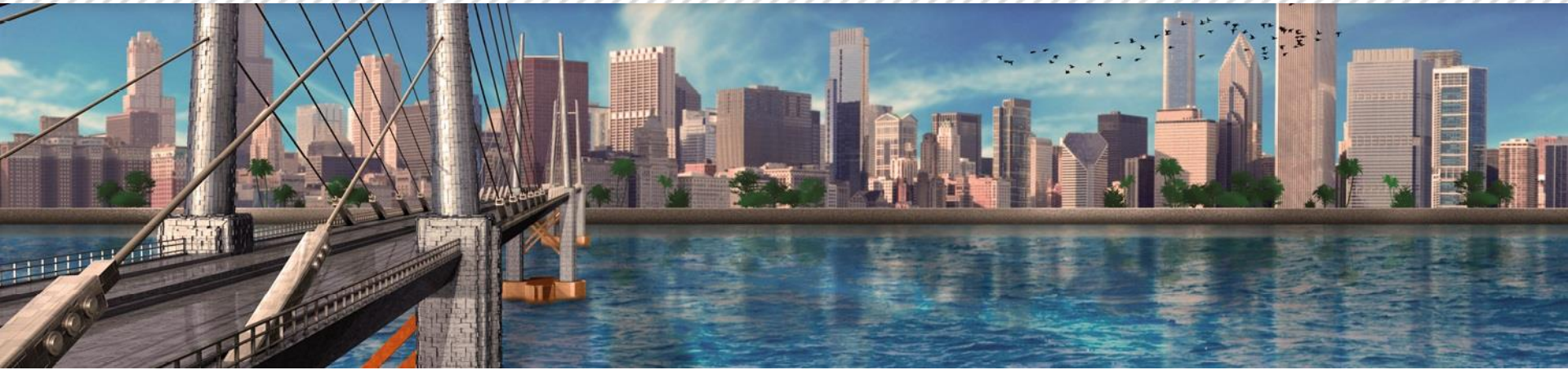


MIT, Nanyang Technological University Singapore

- Low Energy Electronis System, LEES, process
  - FEOL CMOS foundry process
  - III-V integration processing at research lab
  - BEOL CMOS processing

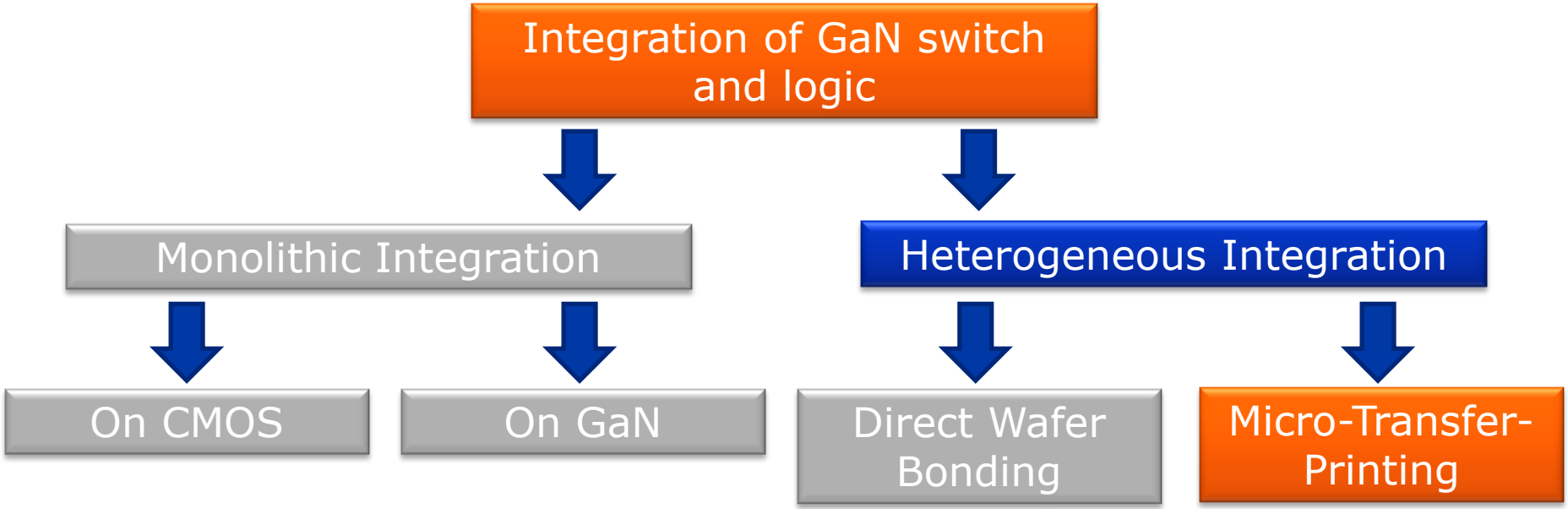


Pilsoon Choi et al, "A Case for Leveraging 802.11p for Direct Phone-to-Phone Communications", 2014 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)

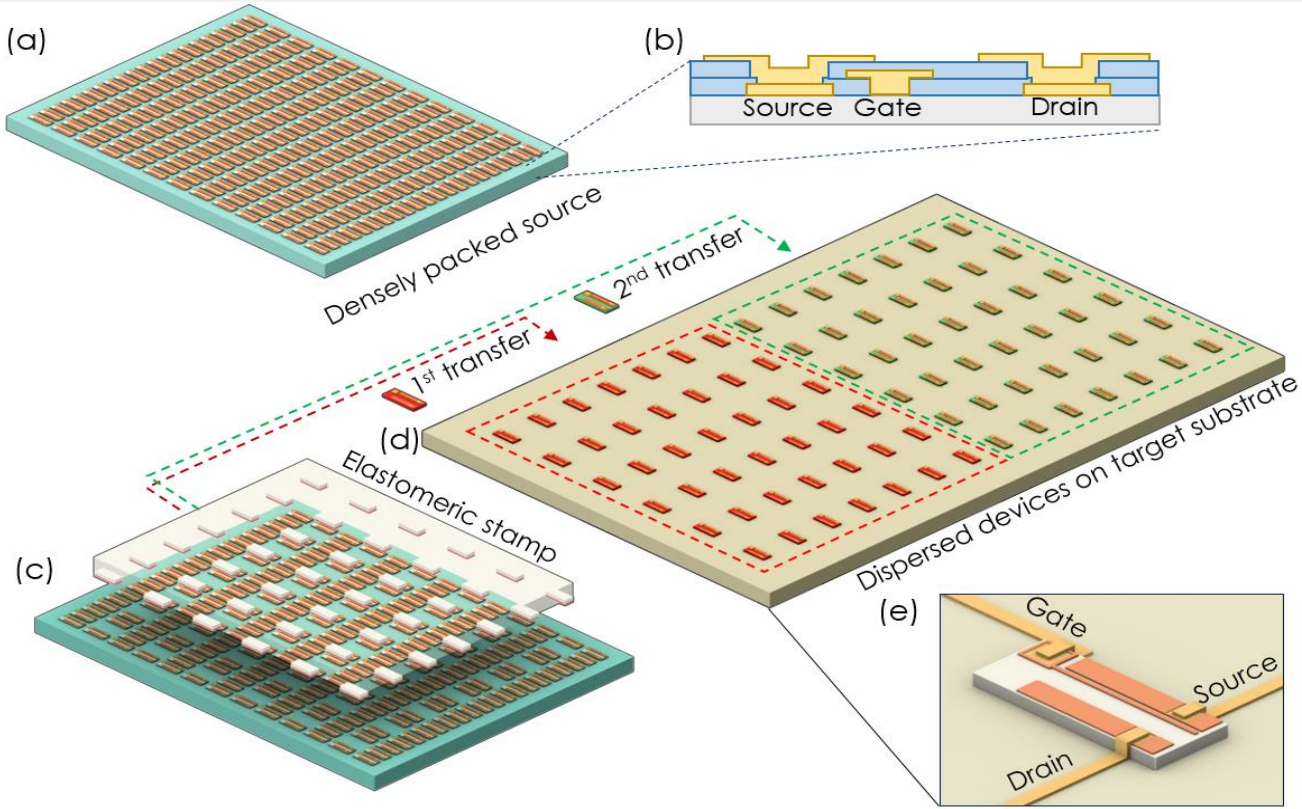


Heterogeneous Integration by micro-Transfer-Printing

Integration variants GaN and CMOS



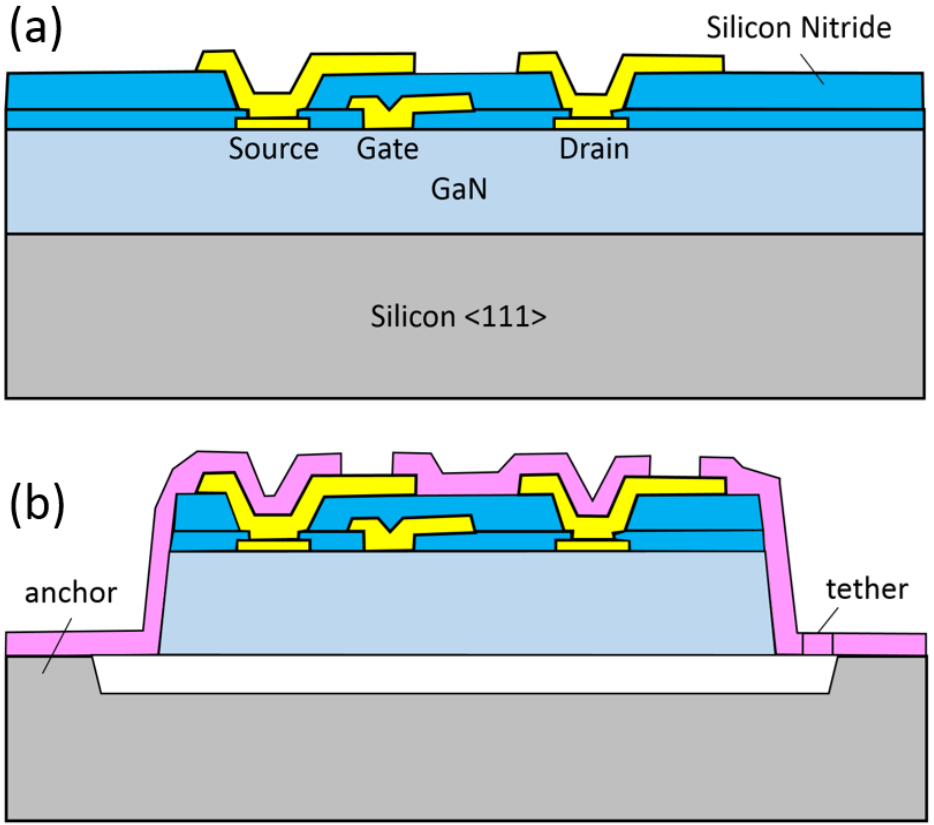
Principle of µTP



R. Lerner et al., "Heterogeneous Integration of Microscale Gallium Nitride Transistors by Micro-Transfer-Printing," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 1186-1189

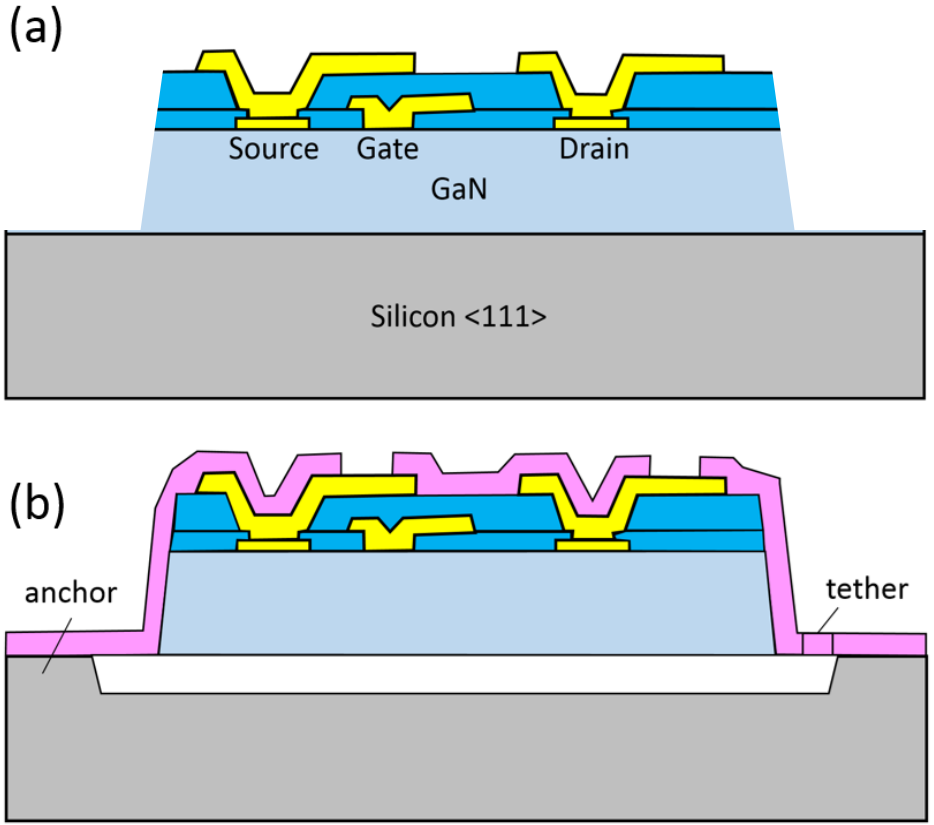
Printable HEMTs

- Trench etch

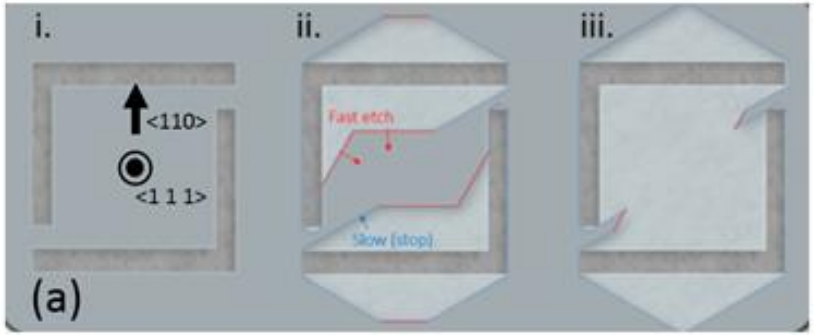


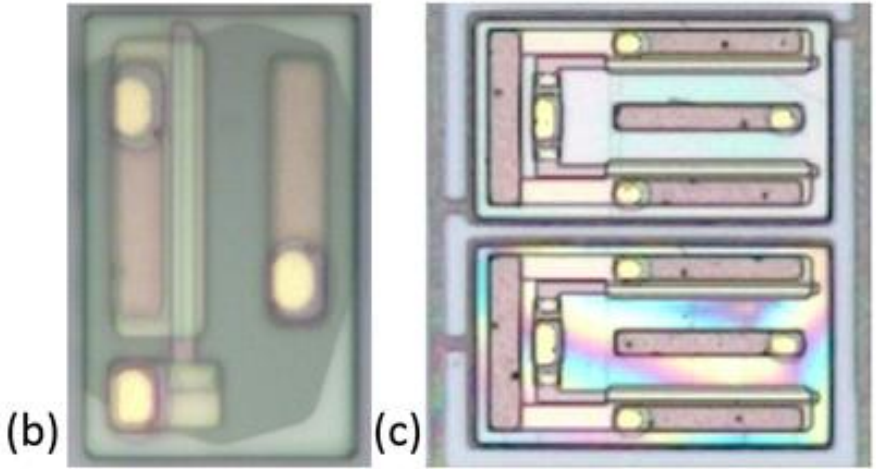
Printable HEMTs

- Trench etch
- Anchor and tether formation
- Release etch



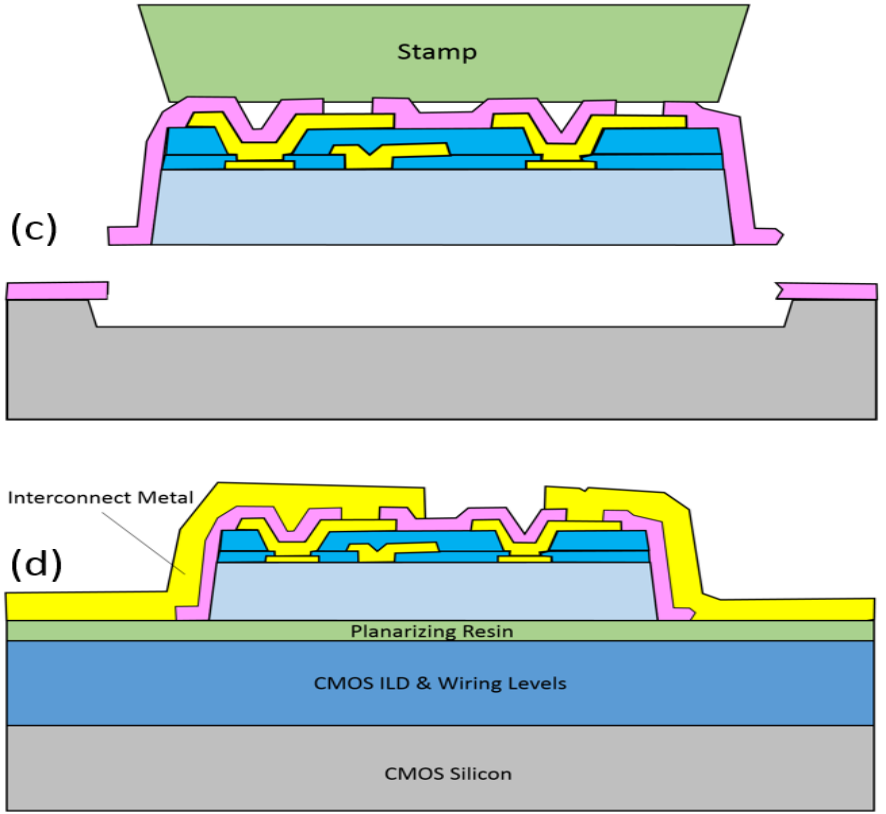
Wet etching for HEMT release



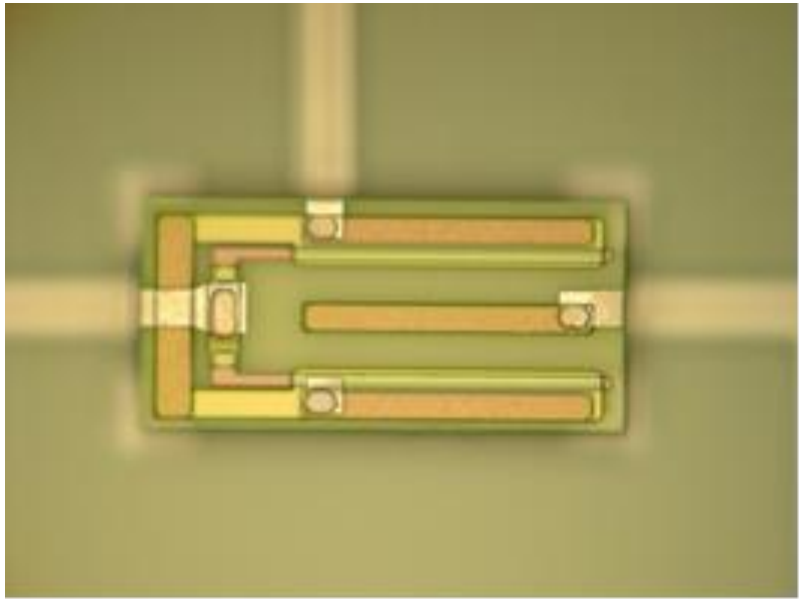


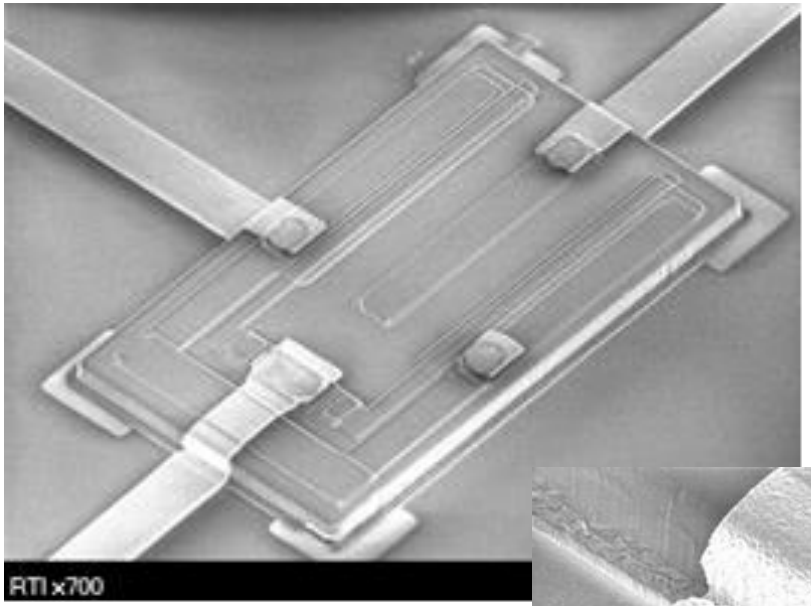
Printing

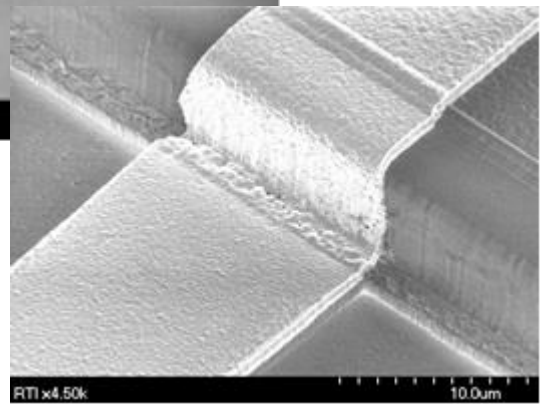
- Printing with elastomeric stamp
- Adhesion between stamp and chip depends on speed
  - Fast: high adhesion for removal
  - Slow: weak adhesion for printing



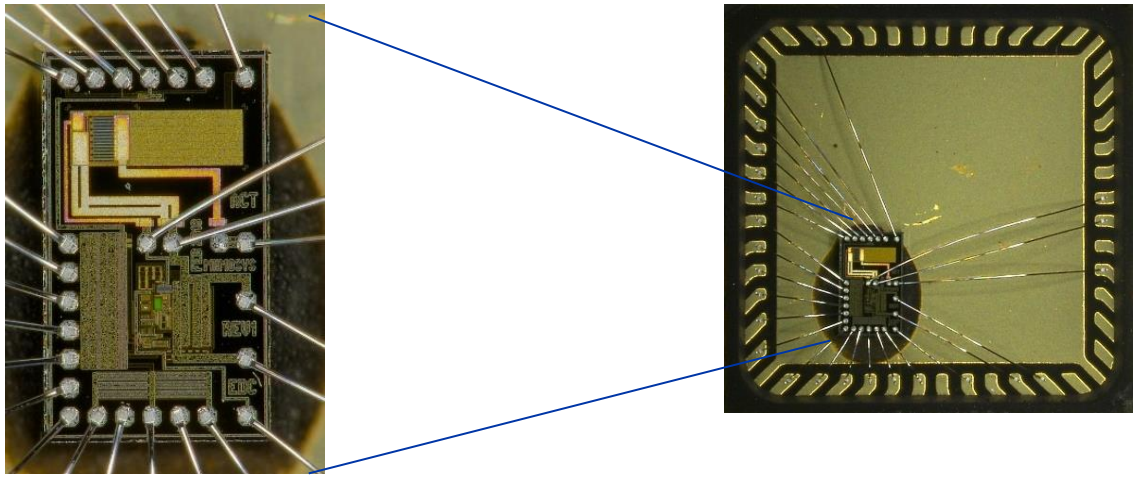
On-wafer metallization







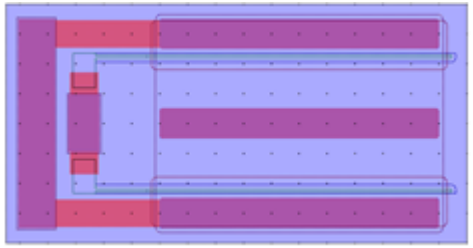
Driver with printed HEMT

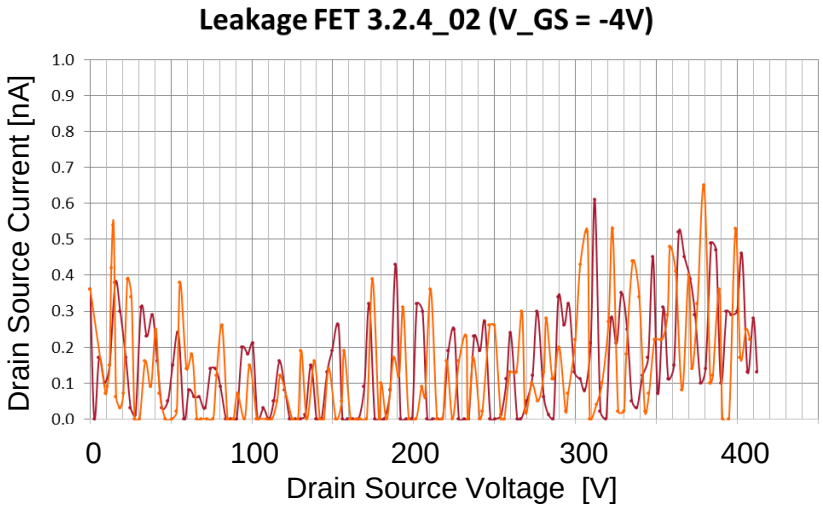


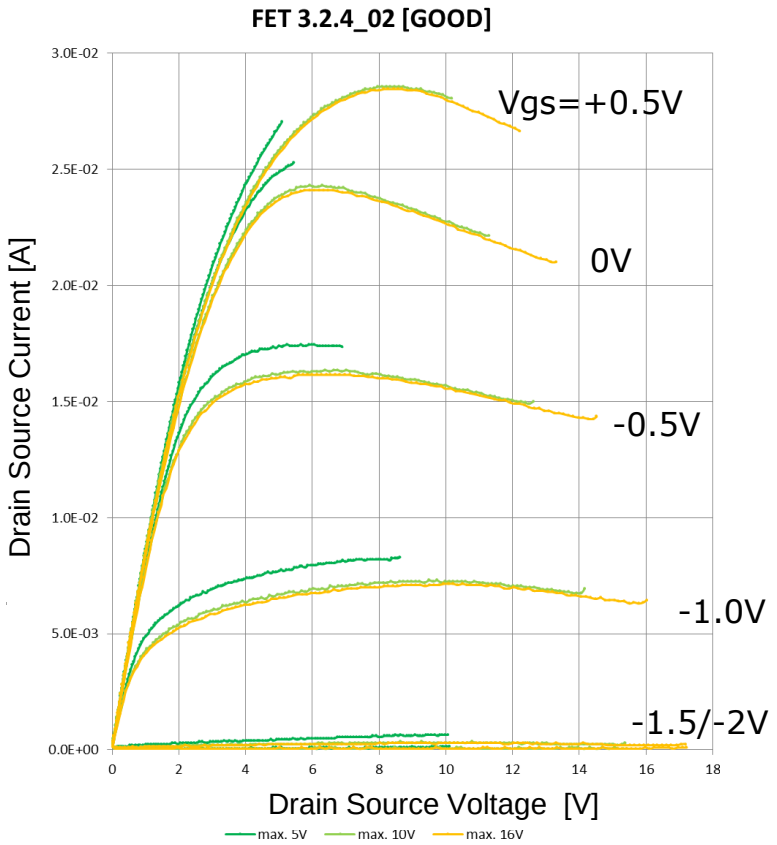
- Driver IC: Electronic Design Chemnitz, EDC
- Driver Process: X-FAB
- HEMT: Fraunhofer IAF Freiburg
- µTP: X-Celeprint
- Asssembly: Turck Duotec

Printed HEMT, electrical results

- W=2*100µm
- Ileak: 1.5pA/µm
- Ids: 135µA/µm

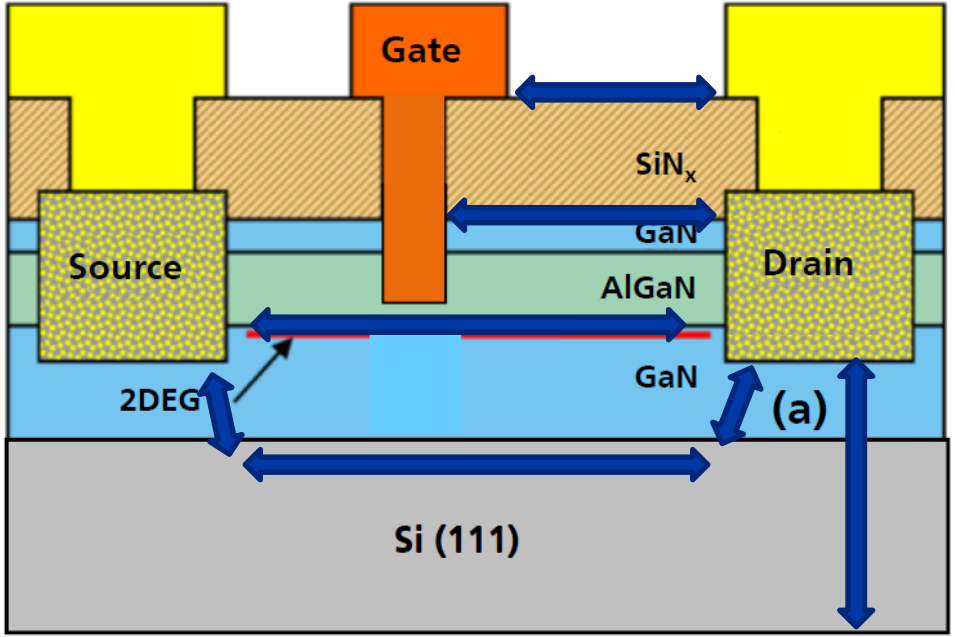




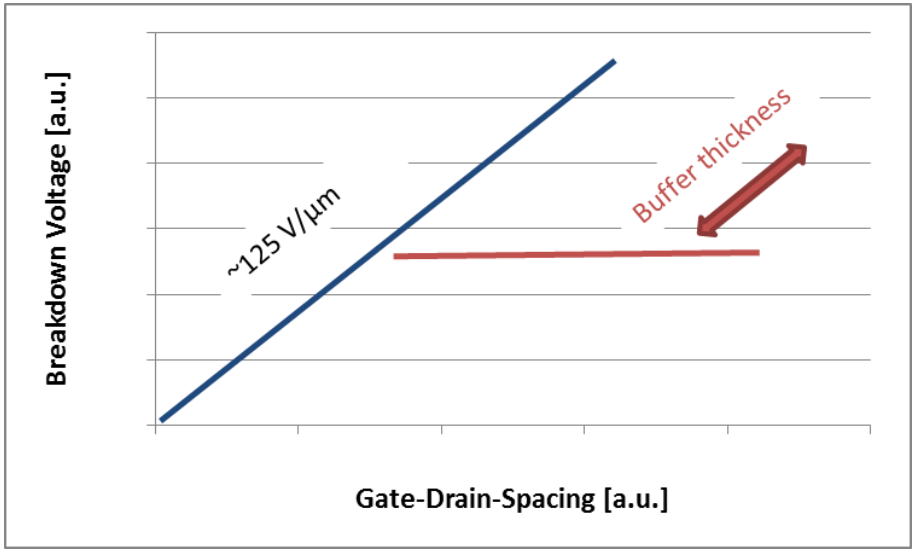


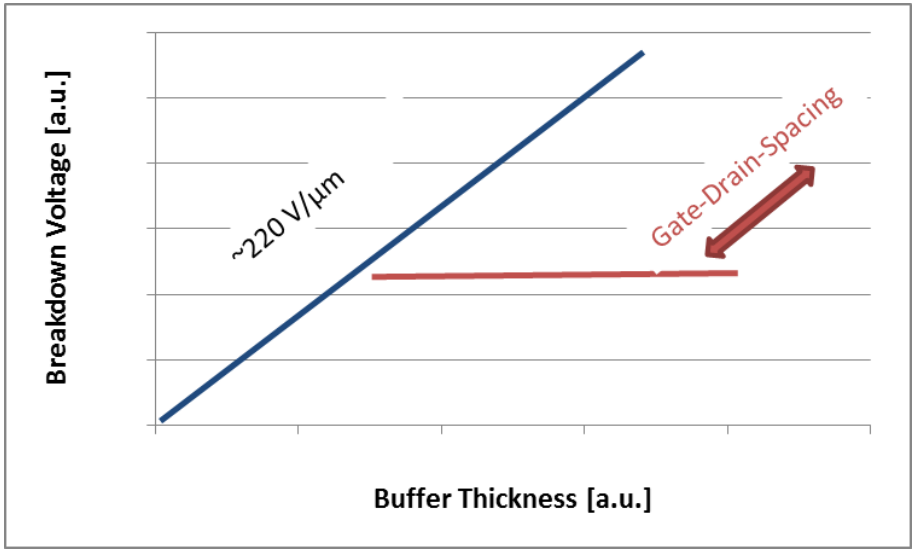
Leakage paths

- Several paths for leakage currents
  - laterally => Gate-Drain spacing
  - but also vertically => buffer thickness
- To reduce leakage through silicon
  - Sufficient buffer thickness
  - => mechanical stress
  - => epi time & costs
  - Main hurdle for >900V GaN HEMTs



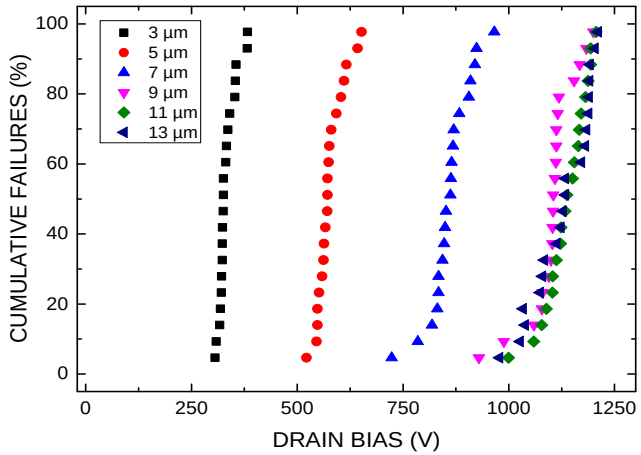
HEMT breakdown - schematic

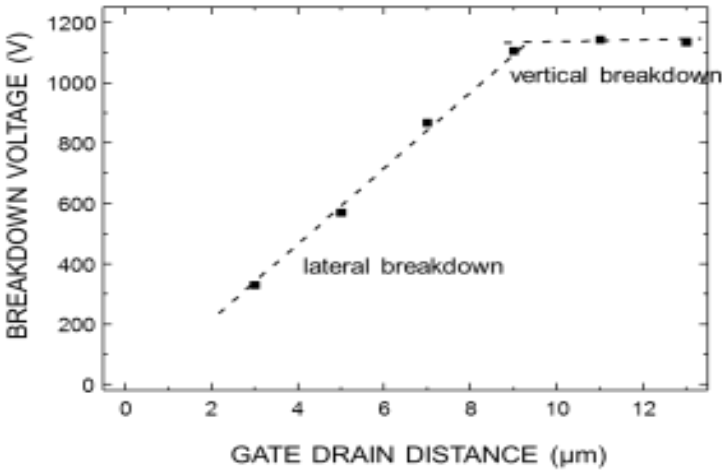




- Lateral breakdown, limited by vertical breakdown
- Vertical breakdown, limited by lateral breakdown

HEMT breakdown - real



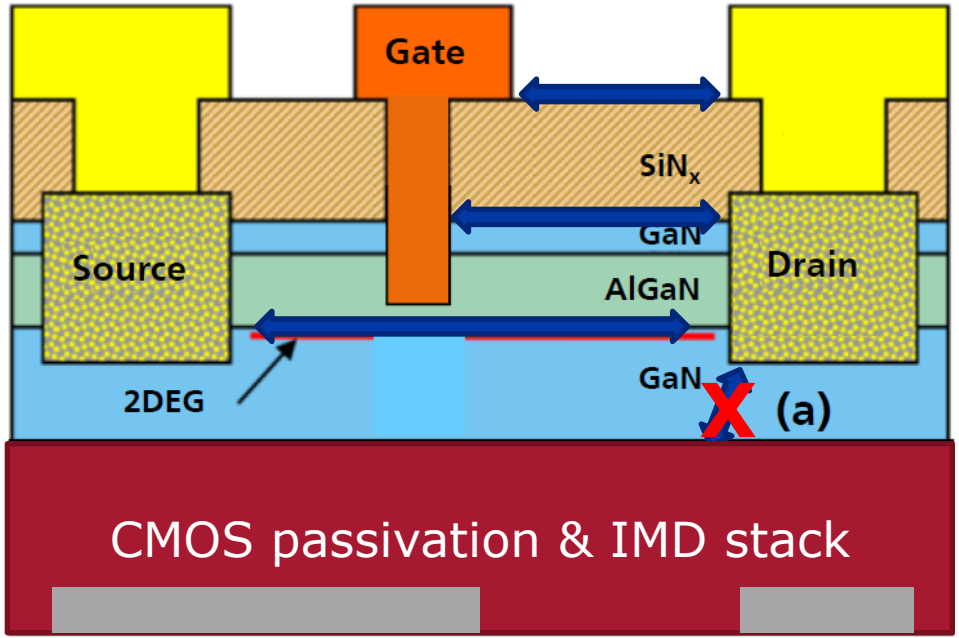


P. Waltereit, et al; Large-area GaN-on-Si HFET power devices for highly-efficient, fast-switching converter applications; in Proc. of the 7th Wide Band Gap (WBG) Semiconductor and Components Workshop 2014, pp.83-88, Frascati, Italy

Leakage paths

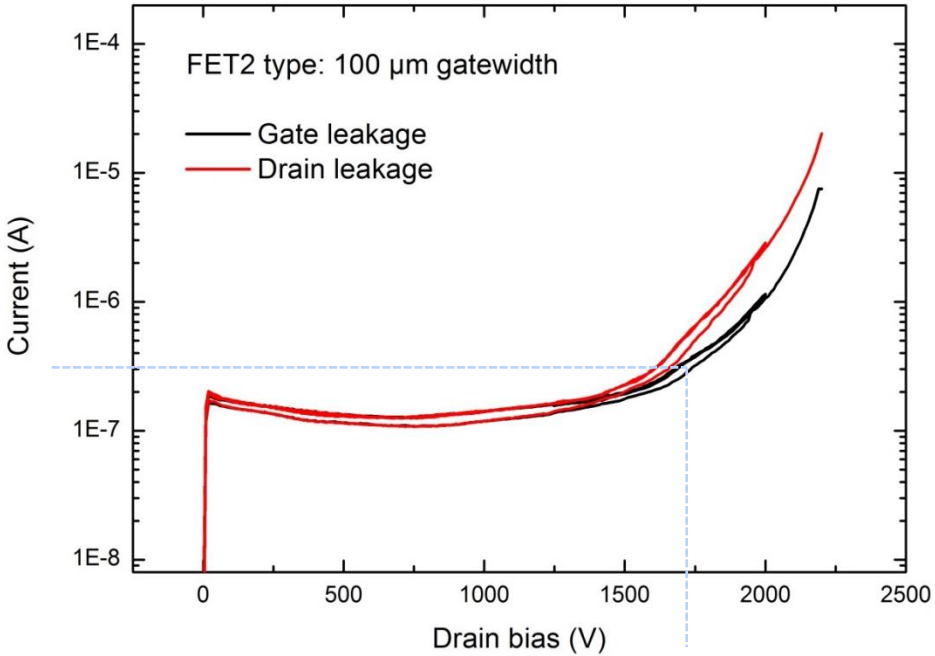
- Several paths for leakage currents
  - laterally => Gate-Drain spacing
  - but also vertically => buffer thickness
- To reduce leakage through silicon
  - Sufficient buffer thickness
  - => mechanical stress
  - => epi time & costs
  - Main hurdle for >900V GaN HEMTs
- With the release etch
  - Silicon removed
  - Replaced by oxide / nitride

also the vertical leakage / breakdown is interrupted



Breakdown behaviour

- 1800V at 1µA drain current with 17µm Gate-Drain spacing
- Breakdown defined (mainly) by the lateral G/D spacing and no longer by the buffer thickness
- Thinner GaN possible



R. Lerner et al., "Integration of GaN HEMTs onto Silicon CMOS by micro Transfer Printing," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 451-454.

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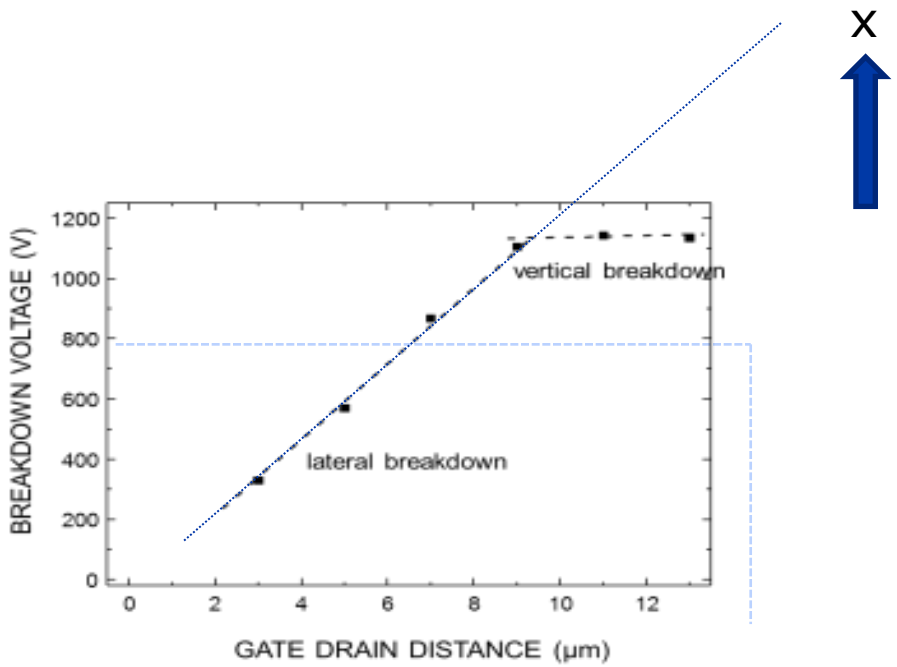
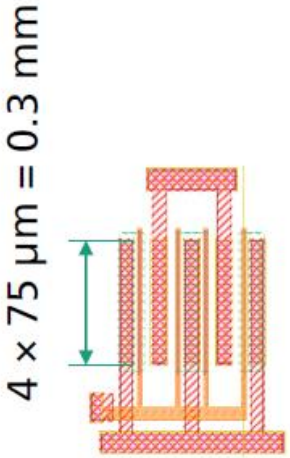
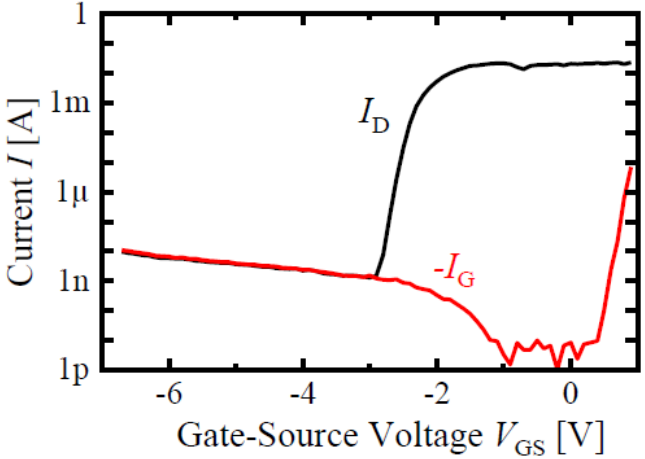
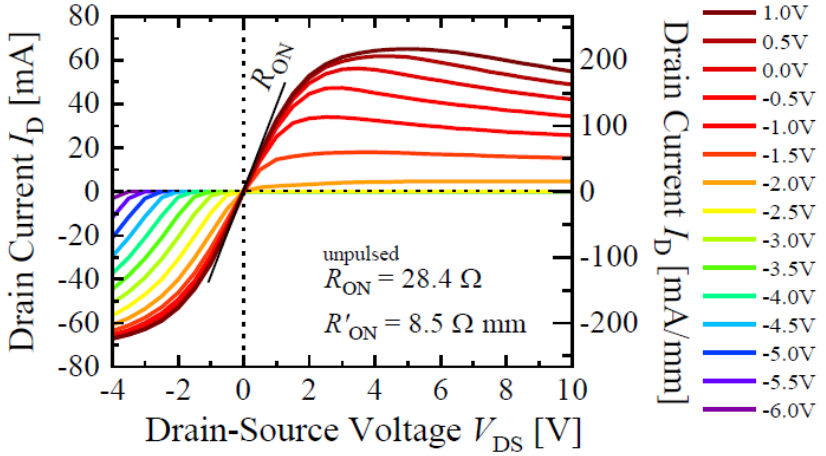


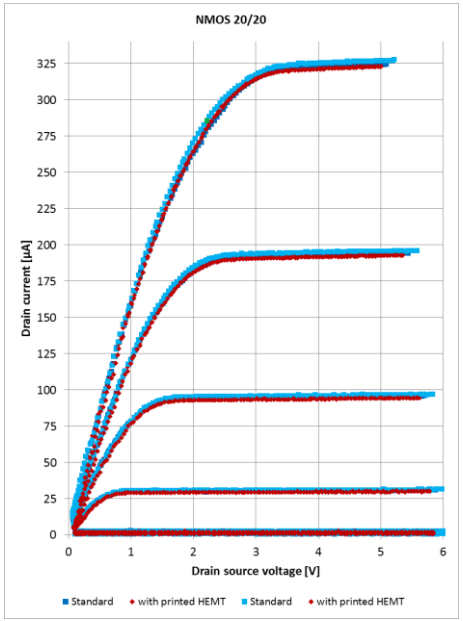
Printed HEMT_4_75_6

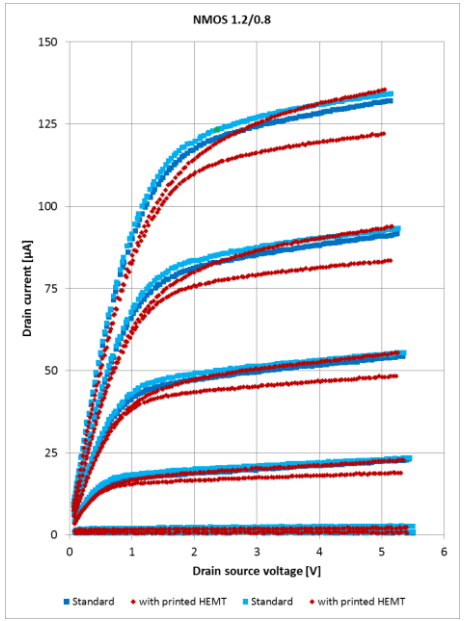


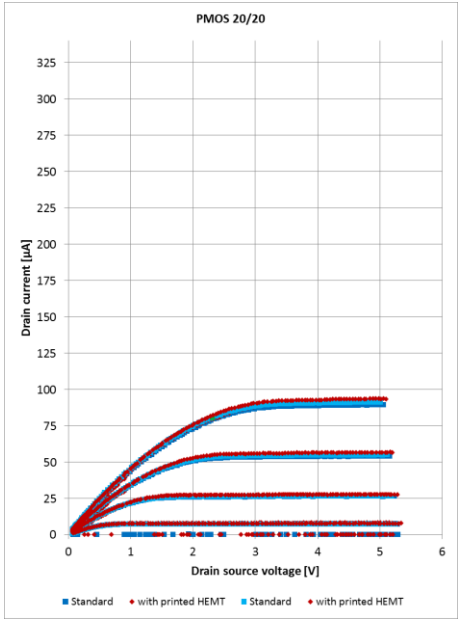


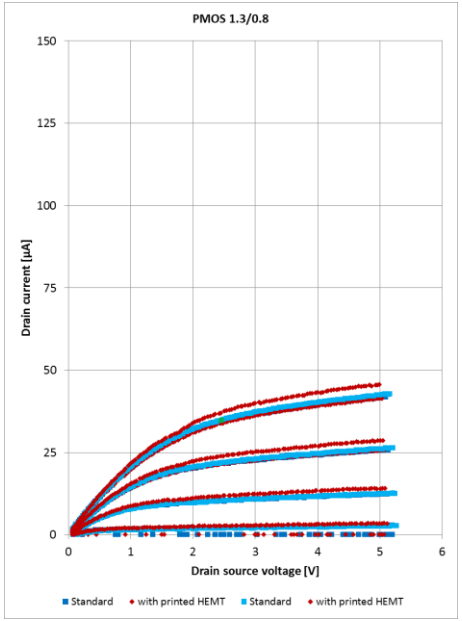


CMOS performance below printed HEMT



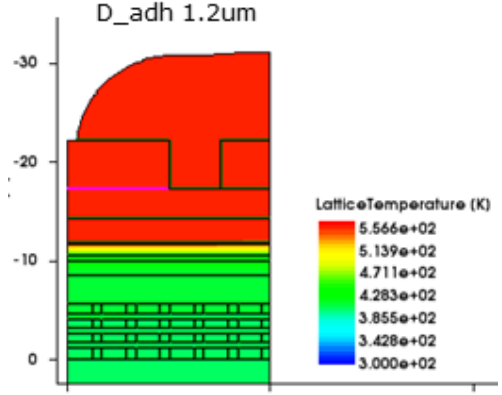






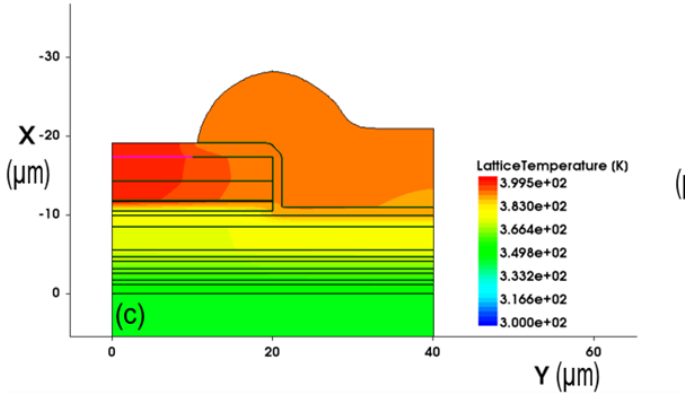
R. Lerner et al., "Integration of GaN HEMTs onto Silicon CMOS by micro Transfer Printing," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 451-454.

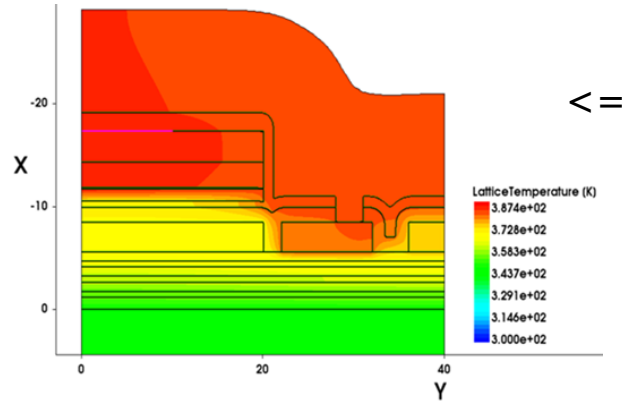
Thermal simulation



<= starting point: 260°C

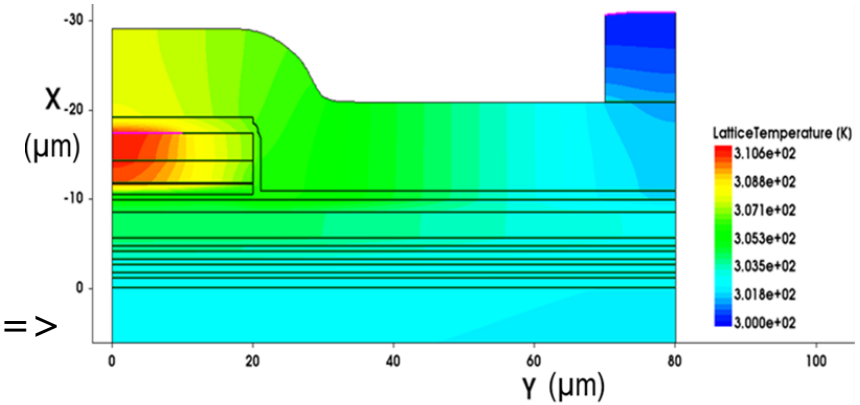
Extension
& thick Cu RDL: 100°C =>





<= cooling
structure: 90°C

Wire bond /
flip chip: 10°C =>



R. Lerner, et al; Flexible and scalable heterogeneous integration of GaN HEMTs on Si-CMOS by micro-Transfer-Printing; Physica status solidi. A 215 (2018), Nr.8, Art.1700556, 7 S.

Challenges

- Several challenges involved
  - Additional process layers for release and interconnect
  - chip positions should fit together; co-design of chips required
- Yield as product of wafer yields and print yield
  - Trade of repair costs versus benefit

Integration by µTP: pros & cons

- Advantages:
  - One chip, ~~one substrate wafer, one process flow~~, one supplier
  - Reduction of assembly effort (less pick & place), reduced number of wire bonds (costs, inductance & reliability!)
  - Reduced footprint
  - Lower costs especially on system level
  - Usage of optimized process flows
- Drawbacks
  - ~~Complex process (crystal orientation, thermal budget, thermal stability)~~
  - ~~Mixed materials monolithic integration: contamination, mechanical and optical parameters~~
  - ~~Partitioning versus current trade-off~~
  - Multiplication of yield numbers
  - Additional process steps

Summary

Monolithic integration on GaN

- Already manufactured
- E.g. 650 V process with 650 V and 100 V HEMT designs
- Some basic electric elements can be done
- But far away from CMOS functionality

Monolithic integration on silicon

- Main challenges related to material differences
  - MOCVD growth temperature
  - CMOS on (100) versus GaN on (111)
- Partitioning problem
  - Only dedicated applications
  - Reduced commercial pressure to find solutions
- At research level

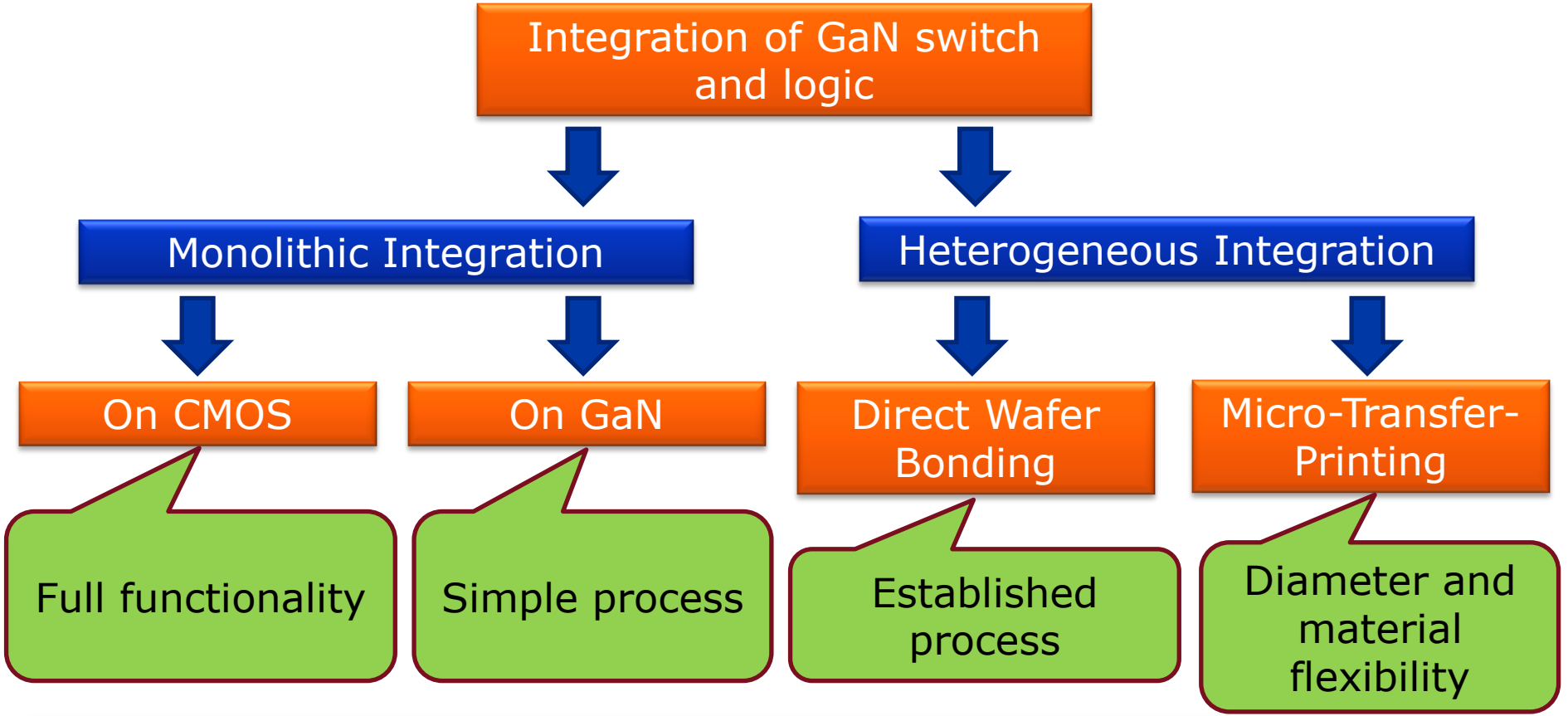
Heterogeneous integration by Direct Wafer Bonding

- 3D stacking and wafer bonding established technologies
- Several challenges
  - Surface flatness
  - Alignment
  - Interconnects
  - Yield multiplication
  - Co-design
- Several limitations
  - Wafer diameter
  - Current through interconnects

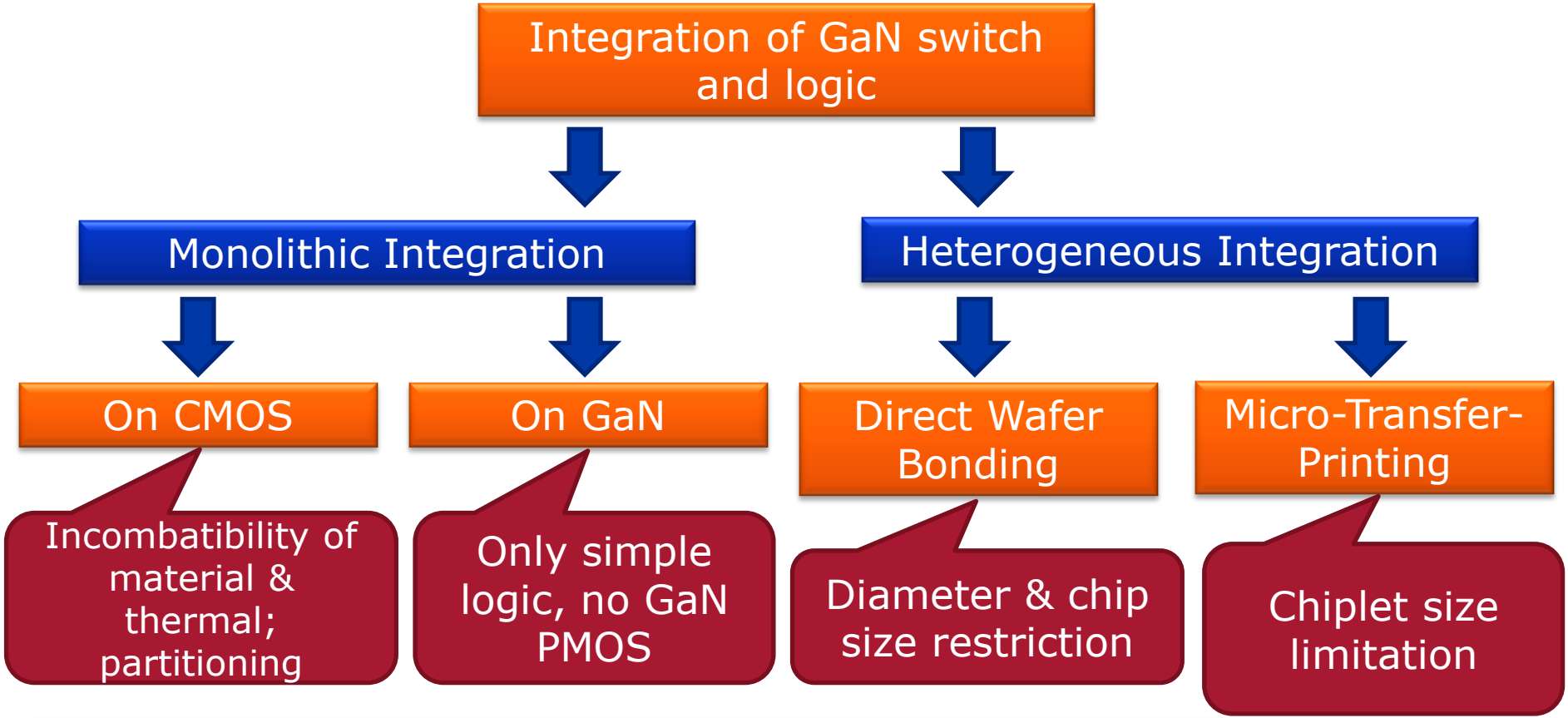
Heterogeneous integration by micro-Transfer-Printing

- Several challenges
  - Yield multiplication
  - Co-design
- Several limitations
  - Only small chiplet size for release

Integration variants



Integration variants



Acknowledgements

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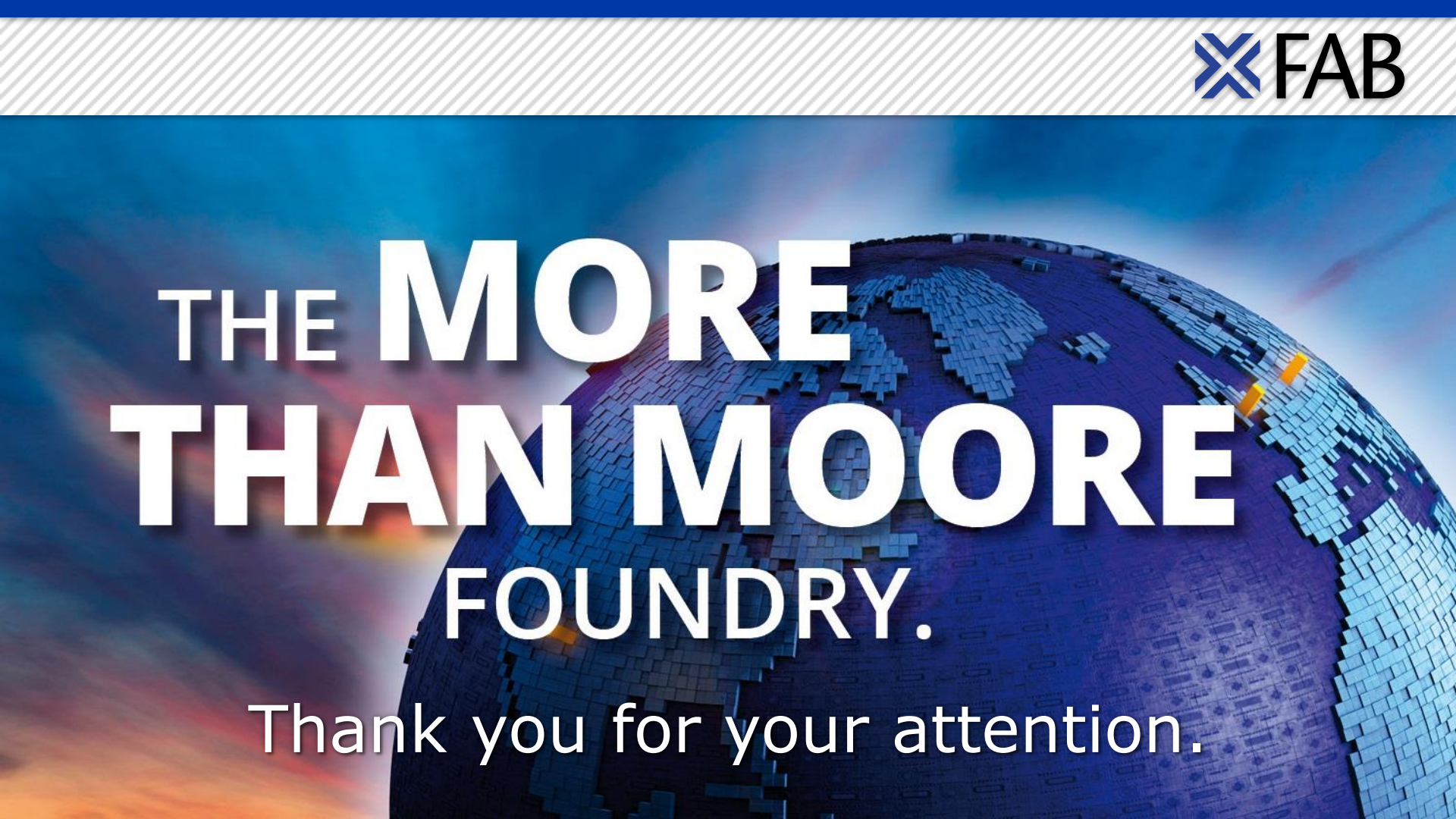
- MIIMOSYS, 16ES0668K,

- ZuGaNG, 16ES0087


FAB
THE MORE THAN MOORE FOUNDRY.
Thank you for your attention.