Printing GaN HEMTs onto silicon CMOS

A micro-transfer printing technique could boost the efficiency of integrated power electronics by uniting high-performance GaN HEMTs with highly integrated silicon CMOS

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LYING AT THE HEART of the majority of today's power ICs are three classes of silicon transistor – those with either a laterally diffused metal-oxide-semiconductor design, an insulated-gate bipolar architecture, or a super-junction configuration. All these workhorses can handle high voltages, high currents, or a combination of both.

It is known from Moore's law that miniaturising these transistors would deliver an evolutionary improvement in performance, but at the expense of spiralling development efforts. Better still is a revolutionary performance gain. This is possible, via the integration of III-V materials.

One of the most promising III-V devices for power electronics is the GaN HEMT. Compared to all forms of silicon device, it sports superior switching speeds, and it also has the upper hand when considering the trade-off between the on-resistance and the breakdown voltage. Thanks to these merits, the GaN HEMT can enable new, highly efficient power conversion topologies that would be unthinkable with state-of-the-art silicon based devices.

Let's not write silicon off just yet, however. Note that bipolar-CMOS-DMOS and high-voltage CMOS technologies have realised high levels of diversification, leading to the highest design complexities. These devices can be used in Smart power ICs, which enable an interface between digital control logic and the power load. By using monolithic integration to position output power devices next to digital and analogue circuitry, it is possible to combine signal processing, sensing and protection circuitry on the same chip. Further benefits of this approach are a trimming of the number of interfaces, the volume, and electromagnetic interferences. The upshot is increased efficiency, performance and reliability.

Engineers working with compound semiconductor technologies are also trying to realise the high-level of functional integration seen in these silicon-based, Smart power ICs. Several technologies for integrating GaN HEMTs with digital and analogue circuitry are currently being pursued: GaN-based Smart power ICs; monolithic integration of GaN on silicon; wafer bonding of GaN on silicon; and the approach that we are investigating at X-FAB Semiconductor Foundries of Erfurt, Germany: heterogeneous integration, enabled by micro-transfer-printing (see Figure 1).

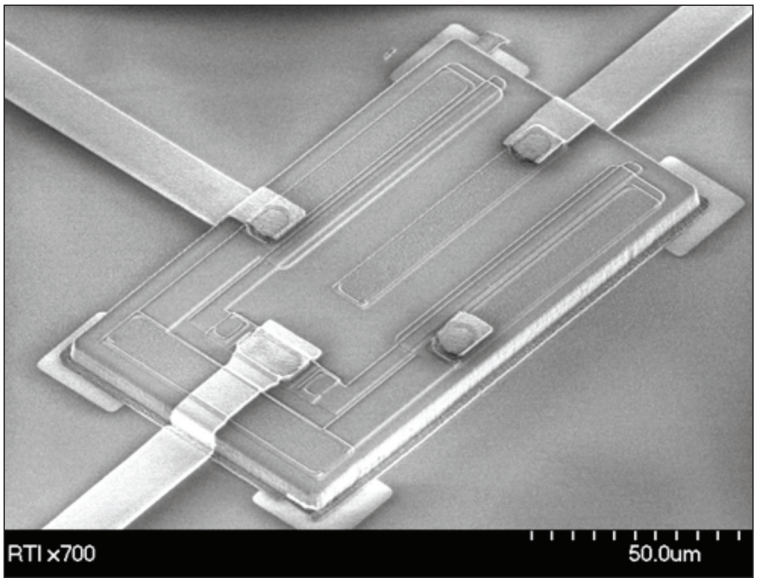


Figure 1. Micro-transfer-printing can position a GaN HEMT on a silicon CMOS wafer, prior to subsequent on-wafer metallization.

Rival approaches

Several groups are working on integrating GaN power devices with GaN digital and analogue circuitry on the same substrate. The downside of this approach is the lack of feasibility of standard silicon-CMOS-like circuit topologies, due to an inferior hole mobility and the absence of high-performance *p*-channel GaN devices. Due to these weaknesses, it may take years to realise high integration densities and functional diversification with GaN-based logic.

Monolithic integration of GaN and silicon CMOS is another option for uniting GaN-based transistors with CMOS logic. Both devices can be fabricated on the same silicon substrate, with custom silicon-on-insulator wafers providing tiers for each technology:

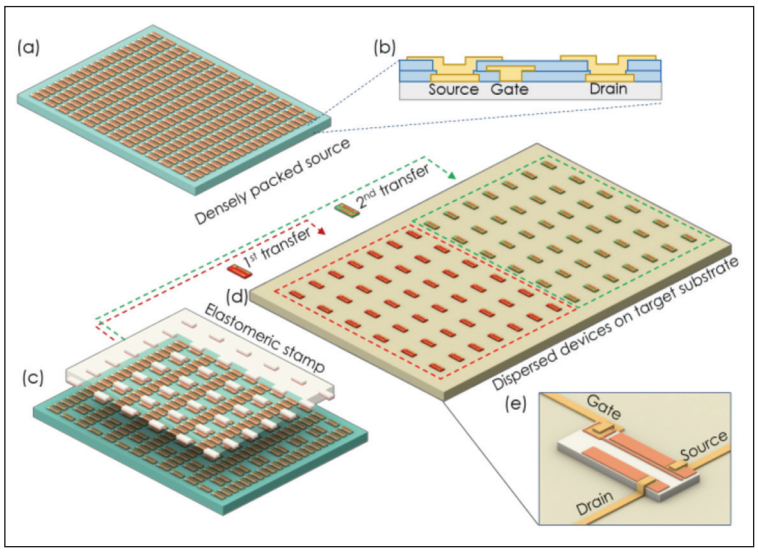


Figure 2. An overview of the micro-transfer-printing process for GaN HEMTs. (a) Source wafer with dense array of HEMTs, (b) HEMT cross-section, (c) elastomeric stamp removes an array of HEMTs from source wafers, (d) first and second printing process on new target substrate, for example a CMOS Wafer, (e) wiring of printed GaN HEMT on wafer.

<100> oriented silicon for CMOS and <111> oriented silicon for GaN. The GaN and silicon transistors are not vertically integrated, but are arranged laterally side-by-side.

A team from Raytheon has pioneered this approach. To reduce the thermal budget, they deposited the GaN layers by MBE, rather than MOCVD. The price to pay for this is a lower throughput, making this approach unfavourable for mass production of higher voltage devices, which require thicker buffer layers.

Additional drawbacks of this approach are: material incompatibilities, such as significant differences in lattice constants and thermal expansion coefficients; device constraints, such as thermal budgets and the restriction of contact metallization materials to CMOS-compatible metals; and high costs. Note that due to the partitioning issue associated with monolithic integration, costs can skyrocket. For example, for an integrated circuit with a total area of 10 mm² – comprising 9 mm² of logic and 1 mm² of GaN HEMT – the costs for the epitaxy process are similar to those for a full-wafer process, but the epitaxial layer is only used on the 1 mm² GaN area. Thus, the costs per GaN area, and also the costs per Amp, are ten times higher.

Another option for combining the merits of GaN power devices with those of silicon CMOS is to fabricate each in its dedicated manufacturing environment, before uniting them densely at the chip level. With this approach, every device is designed to its full potential, irrespective of material and processing constraints. That's because integration takes place by wafer bonding in a post-process step.

We have been pursuing this type of approach through a multi-partner project GaNonCMOS, funded by the European Union's Horizon 2020 Research and Innovation programme. Supported by 7.4 million of investment, this effort that kicked-off in January 2017 is aiming to bring GaN power electronic materials, devices and systems to the next level of maturity by providing densely integrated materials. A key goal within the project is to realise long-term reliability improvements over the full value chain of materials, devices, modules and systems.

Micro-transfer printing

One of the key technologies in our project is micro-transfer-printing. Like wafer bonding, it facilitates the post-process integration of GaN power and silicon CMOS devices, but it also allows the deterministic assembly and integration of microscale, high-performance semiconductor devices onto non-native substrates.

The key process with micro-transfer-printing is the picking-up of large arrays of microscale devices from their source wafer with an elastomer stamp, and the subsequent printing of these devices on a retrieving wafer. This is accomplished by housing the stamps

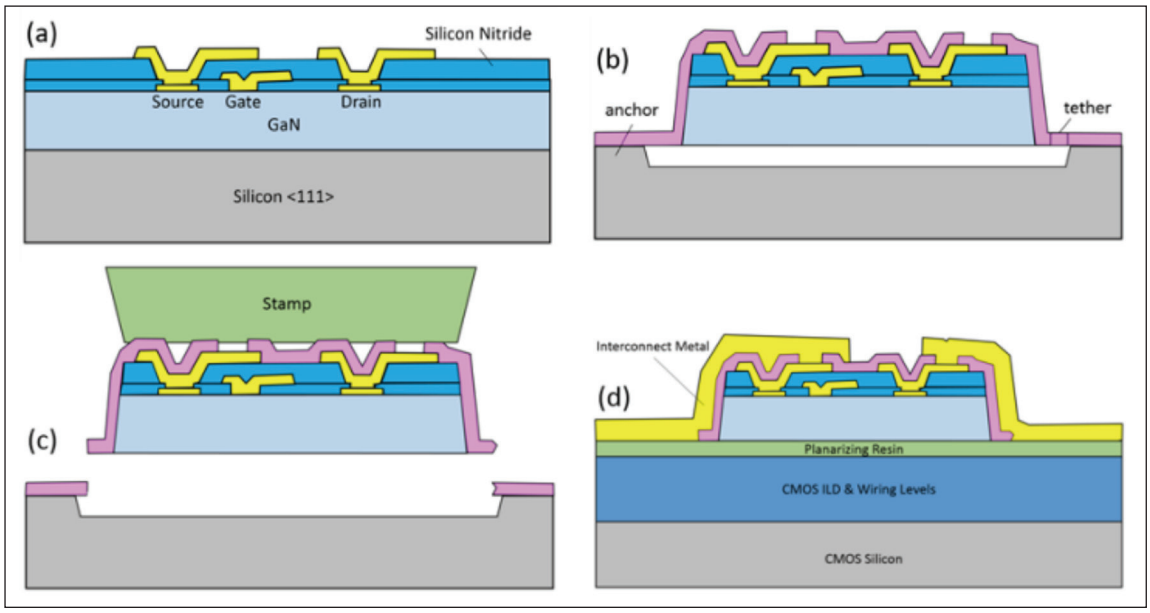


Figure 3. The process flow for heterogeneous integration of GaN HEMTs. (a) The transistors are fabricated on a <111> silicon substrate. (b) The devices are isolated, passivated and then undercut. (c) The devices are retrieved with an elastomer stamp. (d) The devices are printed to a silicon CMOS wafer and then interconnected using thin-film aluminium traces.

on high-precision, motion-controlled print-heads. With this parallel process, many small chiplets carrying GaN HEMTs can be printed onto fully processed silicon CMOS wafers in one go (see Figure 2).

The majority of GaN HEMTs are grown and manufactured on <111> oriented silicon wafers. To prepare them for the micro-transfer-printing process, these devices then need to be released from their native substrate.

In the project that we are involved with, this step is undertaken by reactive ion etching through the device layers and down to the underlying silicon substrate (see Figure 3 (a)). Then, to passivate the sidewalls and form an anchor that tethers the structures, a SiN layer is added by plasma-enhanced CVD (see Figure 3 (b)).

After this, the <111> oriented silicon underneath the device is wet-etched using a high-selective, anisotropic etchant (see Figure 4 (a)). As the etch rate in the {110} family of directions is more than one hundred times faster than it is in the orthogonal directions, regions where the silicon does not undercut remain as anchors for the release process (see Figure 4(c) for an optical microscope image of two fully undercut, print-ready GaN HEMTs with different tether configurations).

Utilising the viscoelastic nature of the elastomer stamp, GaN devices are then picked-up from their source wafer and printed on the CMOS wafer. Due to the high adhesion between the stamp and the GaN device, when the stamp is then moved rapidly away from a bonded interface, the tethers are broken, enabling the pick-up of microscale devices from their native substrates. A different approach is used to print the devices. This time the stamp is gently moved away from the bonded interface, causing the adhesion between the stamp and the device to be lower than that of the bond forces. Due to this, the stamp separates from the chips, which stick on the new, non-native substrate.

Following the micro-transfer-printing process, interconnections are added with standard wafer fabrication processes, such as thin-film deposition and photolithographic patterning (see Figure 3 (d)). With this approach, which involves on-chip wiring, process temperatures do not exceed 175 °C, permitting the use of complex Smart power designs.

Promising results

Small GaN HEMTs have been manufactured with various gate finger configurations, channel widths and

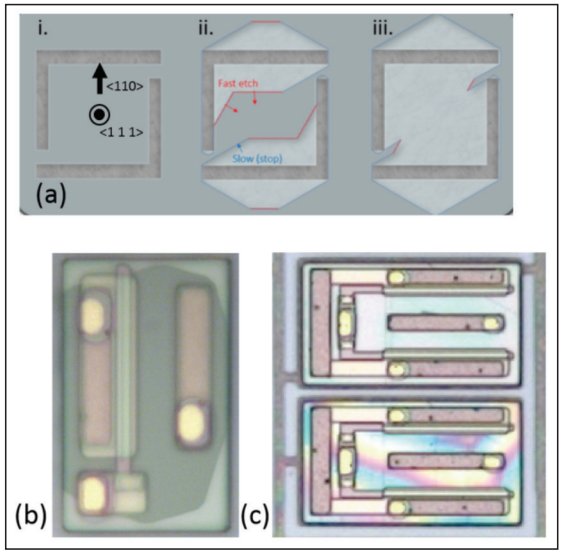


Figure 4: (a) Silicon <111> wet-etching underneath a device. (b) The etch-fronts can be seen by looking through a GaN HEMT that is only partially etched. (c) Optical micrograph of GaN HEMTs that have been fully undercut, with two different tether designs.

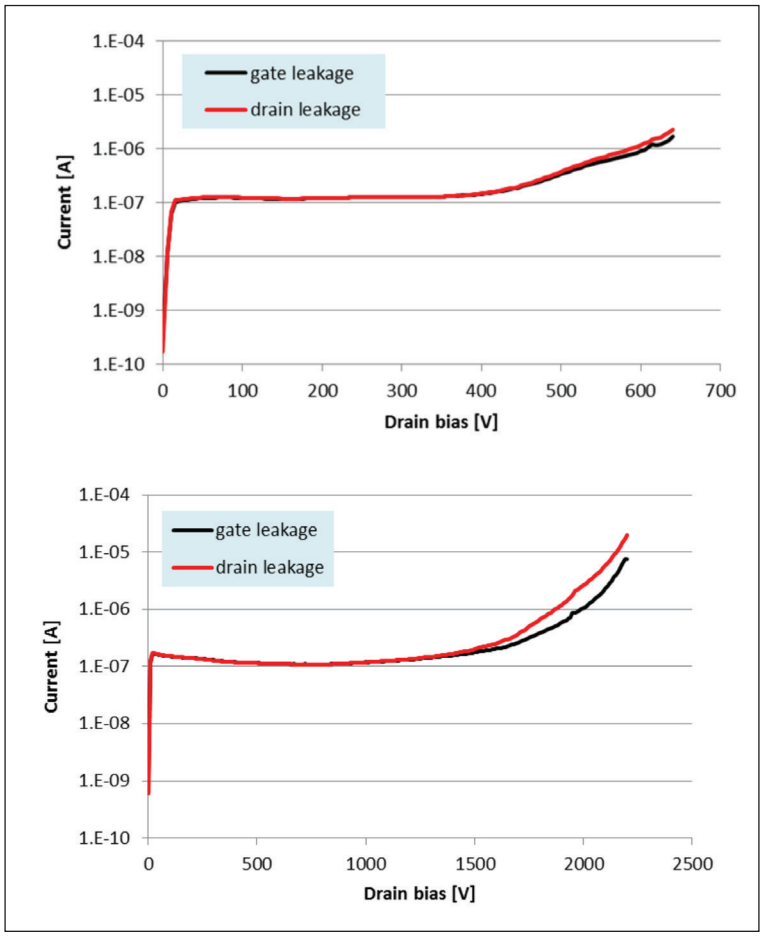


Figure 5: Blocking characteristic of HEMT with gate-to-drain distances of 6 µm (top) and 17 µm (bottom).

gate-to-drain spacings (see Table 1 for an overview). All of these HEMTs have been produced with the same set of processes, and made from the same substrate wafer, which features a GaN epitaxial structure that is about 4 µm-thick. Using the processes described above, the HEMTs have been transferred to two types of wafer: completely processed silicon CMOS wafers; and trench-isolated, silicon-on-insulator high-voltage CMOS wafers.

The benefits of printing HEMTs directly on top of CMOS are not limited to a smaller footprint for the final device – they also enable shorter wiring between the logic and the HEMT, reducing parasitic inductances and capacities (see box "Strengths of micro-transfer-printing" for a detailed list of benefits).

Initial results include characteristics for a 20 V NMOS transistor that are undisturbed by the printed HEMT, and promising room-temperature, drain-source blocking mode characteristics for the printed GaN HEMT device (see Figure 5). Using a fluorinert protection layer to avoid surface flash overs and premature breakdowns, printed HEMTs have achieved blocking voltages of between 600 V and 1800 V, dependent on the drain-gate spacing.

During the release etching, the conducting silicon substrate is removed, allowing the printing of the HEMT on top of the isolating CMOS dielectric. This eliminates a vertical leakage path through the silicon, and it restricts the breakdown mechanism, so that

Gate fingers	Total gate width [µm]	Gate-Drain spacing [µm]	Active device area [µm²]	Printed device area [µm²] *)
1	50	17	2279	4956
1	50	6	1696	3983
1	100	17	4429	7614
1	100	6	3296	6063
2	150	17	5694	12264
2	150	6	3978	9052
2	200	17	7519	14280
2	200	6	5253	10540
4	300	17	10374	24675
4	300	6	6942	21000

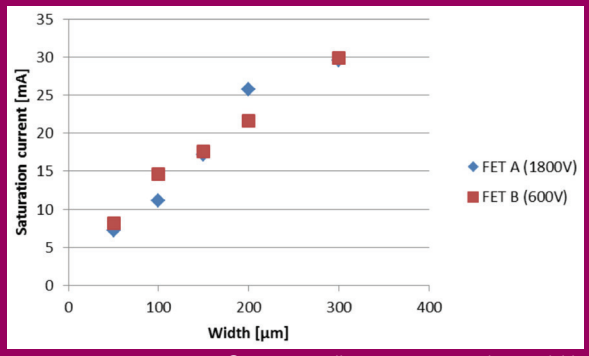
*) including gate pads, source finger shorts etc.

Table 1: GaN HEMT geometry overview

Strengths of micro-transfer-printing

THERE are many merits associated with micro-transfer-printing:

- The GaN buffer thickness can be significantly thinned without sacrificing the breakdown voltage of the printed devices
- Growth times for the GaN buffer can be shorted, and the related mechanical stress issues can be reduced.
- With thinner GaN, the topology step is decreased when routing the printed HEMTs on the surface i.e. when a metal track has to bridge the printed HEMT's edge.
- A scaling of the breakdown voltage with gate-drain distance enables the manufacture of GaN devices with different breakdown voltages in the same process, and even on the same wafer.
- A scaling of the on-state parameters on-resistance and saturation current is possible with the designed channel width (see figure on the right)
- By removing printing-related mechanical design restrictions, the placement of the printed HEMTs can be realised relative to certain logic blocks. For example, a very close proximity of HEMT and cascode NMOS or gate driver circuitry below the HEMT can be realized.



Current scaling versus transistor width for GaN HEMTs in two voltage classes

breakdown only occurs laterally in the GaN. Due to this, the breakdown voltage is solely determined by the gate-drain distance.

Another task undertaken has been to carry out a thermal TCAD Design of Experiment, in order to identify the main contributors to the thermal resistance of GaN HEMTs printed on top of a CMOS circuit. This effort revealed that there is only a small increase in the thermal resistance due to the CMOS dielectric layers – it is far less, for example, than the thermal contribution of wafer and metallisation thickness. Under AC conditions the thickness of the HEMT has a larger effect on the thermal resistance than the CMOS dielectric layers. Consequently, if silicon is removed in the manner that we have described, along with possible thinning of the GaN buffer layers, the CMOS oxide layers do not increase the total thermal resistance.

The results detailed here have been achieved within device level investigations. The next steps will be undertaken in an ongoing project MIIMOSYS, funded by the German ministry for education and research.

This project – involving Electronic Design Chemnitz GmbH, Fraunhofer Institute for Applied Solid State Physics, TURCK duotech GmbH (TDU), University of Erlangen-Nuremberg, Chair of Electron Devices, and X-FAB Semiconductor Foundries with support from X-Celeprint – is targeting the first ever demonstration of hetero-integrated GaN transistors onto silicon CMOS control electronics at the system level. Topics of future investigations will be the next steps towards a manufacturing process for micro-transfer-printing, the reliability of the involved GaN and CMOS devices and the packaging of micro-transfer-printed devices for bridge drivers and controller ICs for motor and LED driver applications.

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Further reading

T. Erlbacher; "Lateral Power Transistors in Integrated Circuits", Springer, Heidelberg New York Dordrecht London, 2014
"Power GaN Devices", edited by Matteo Meneghini, Gaudenzion Meneghesso, Enrico Zanoni, Springer International Publishing, 2017
"Smart Power ICs", edited by Bruno Murari, Franco Bertotti and Guiovanni A. Vignola, Springer International Publishing, 2002
R. Reiner et al., "Monolithically-Integrated Power Circuits in High-Voltage GaN-on-Si Heterojunction Technology", IEEE, 2016
T. E. Kazior et al., "High Performance Mixed Signal and RF Circuits Enabled by the Direct Monolithic Heterogeneous Integration of GaN HEMTs and Si CMOS on a Silicon Substrate", IEEE, 2011
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